

Enrico/Caruso 15" UMA Schematics Document

Sandy Bridge


Intel PCH

2011-06-02

REV : A00

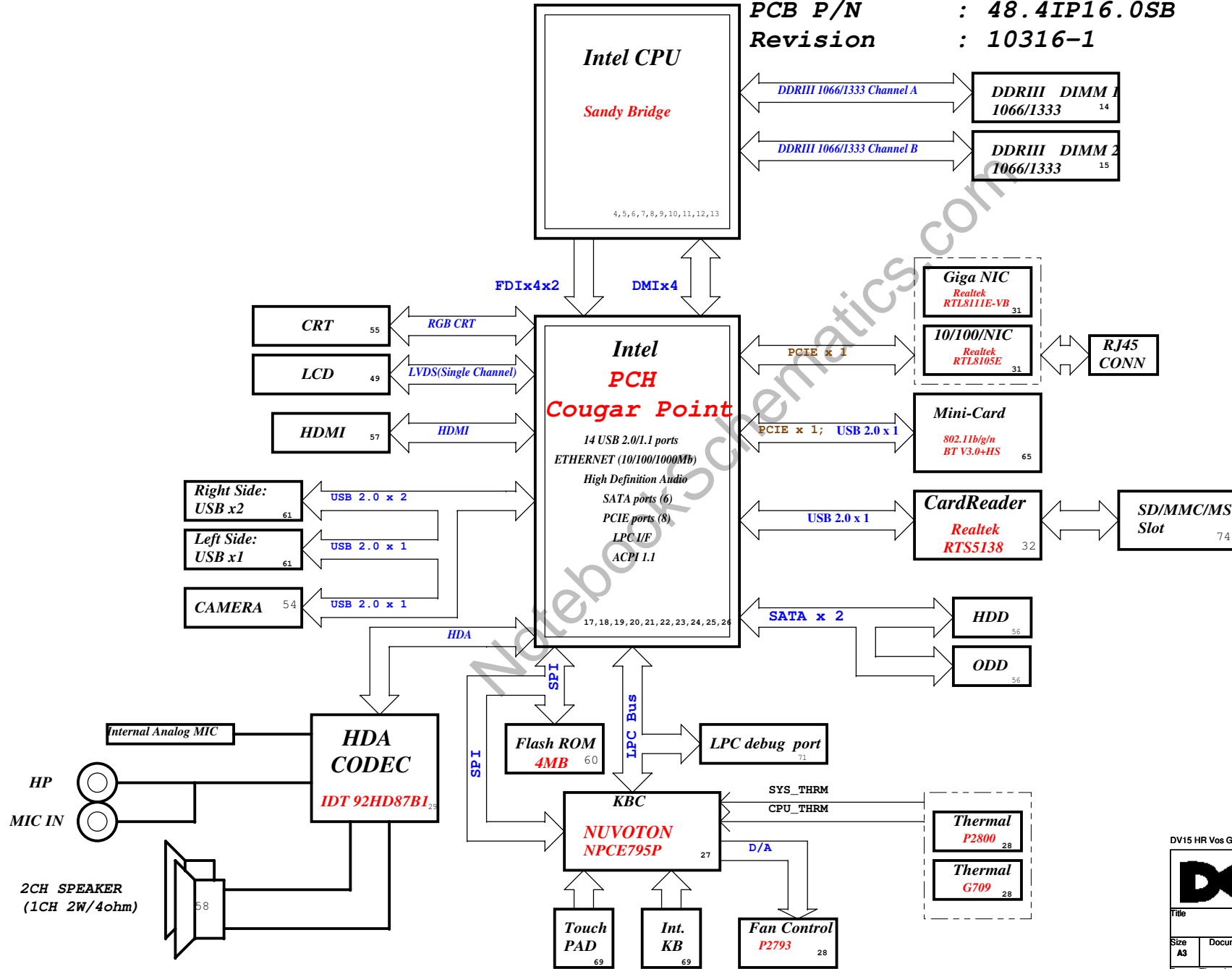
DY :None Installed
PSL:10mW internal schematic
10mW: 10mW schematic installed
Surge: Surege schematic installed
GIGA: GIGA schematic installed
10/100: 10/100 schematic installed
HDMI: HDMI schematic installed
Debug: Debug schematic installed

DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Cover Page		
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DV15 Huron River UMA Block Diagram

Project code : 91.4IP01.001
 PCB P/N : 48.4IP16.0SB
 Revision : 10316-1



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0
CPU DC/DC ISL95831HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
GFX DC/DC ISL95831HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5
SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
MAXIM CHARGER BQ24707 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC TPS51311RGTR 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0
PCB LAYER	
L1: Top	L4: Signal
L2: GND	L5: VCC
L3: Signal	L6: Bottom

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Title: **Block Diagram**

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Enrico/Caruso 15 HR

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

PCIE Routing

LANE1	X
LANE2	Onboard LAN
LANE3	x
LANE4	Mini Card1 (WLAN)
LANE5	X
LANE6	X
LANE7	X
LANE8	X

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Embedded DisplayPort. 0: Enabled - An external Display Port device is connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.05V 0.4 to 1.25V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S9 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-12.6V 9V-19V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN		Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		Ref Des	HURON RIVER ORB Bus	
Device	Address	Hex	Bus	
EC SMBus 1 Battery CHARGER			BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA	
EC SMBus 2 PCH			SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA	
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) MINI			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK	

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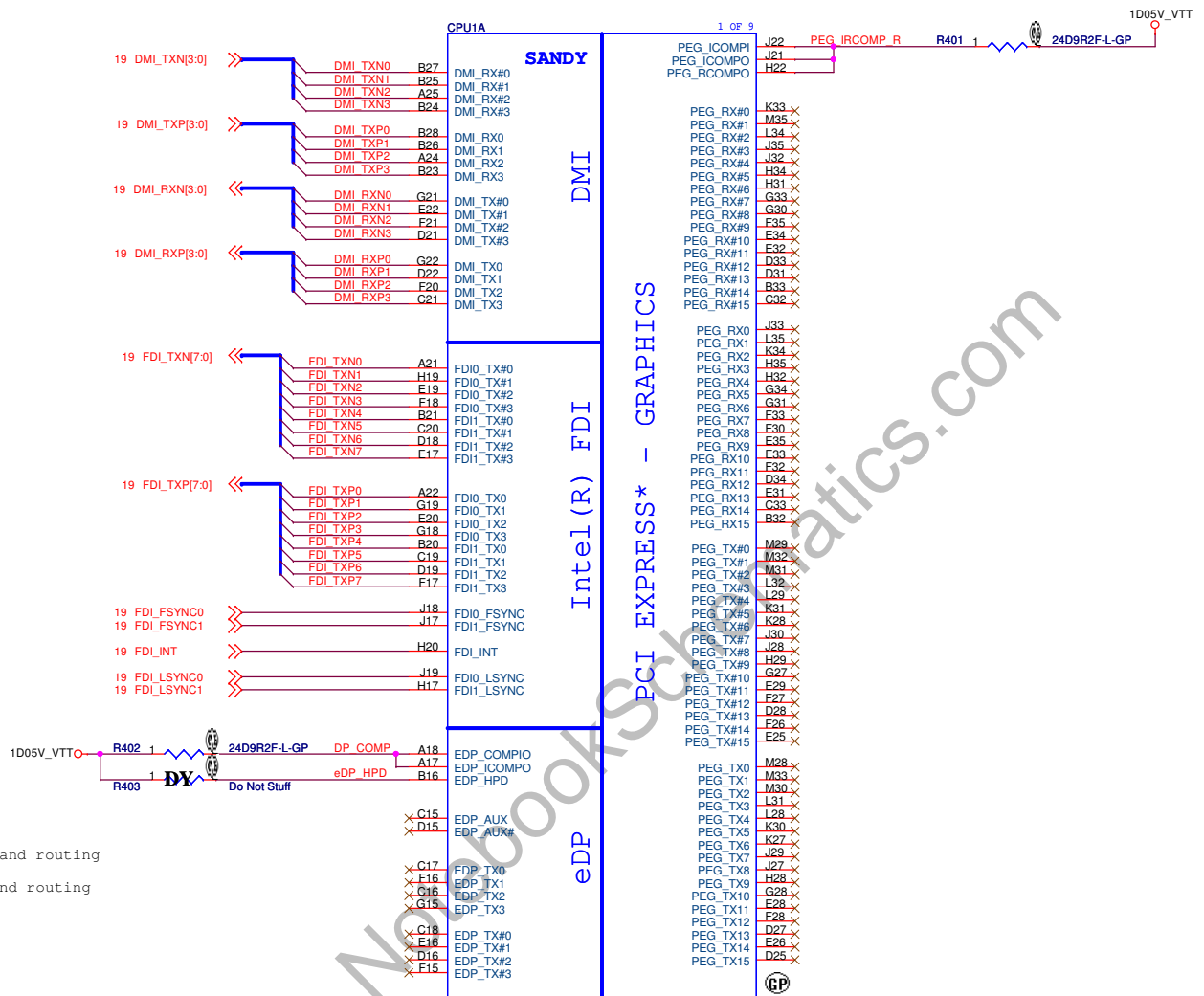
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Table of Content

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCMP1 keep W/S=4/15 mils and routing length less than 500 mils.



SKT-BGA989C468393H184-NF
62.10040.821
2nd = 62.10040.771

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

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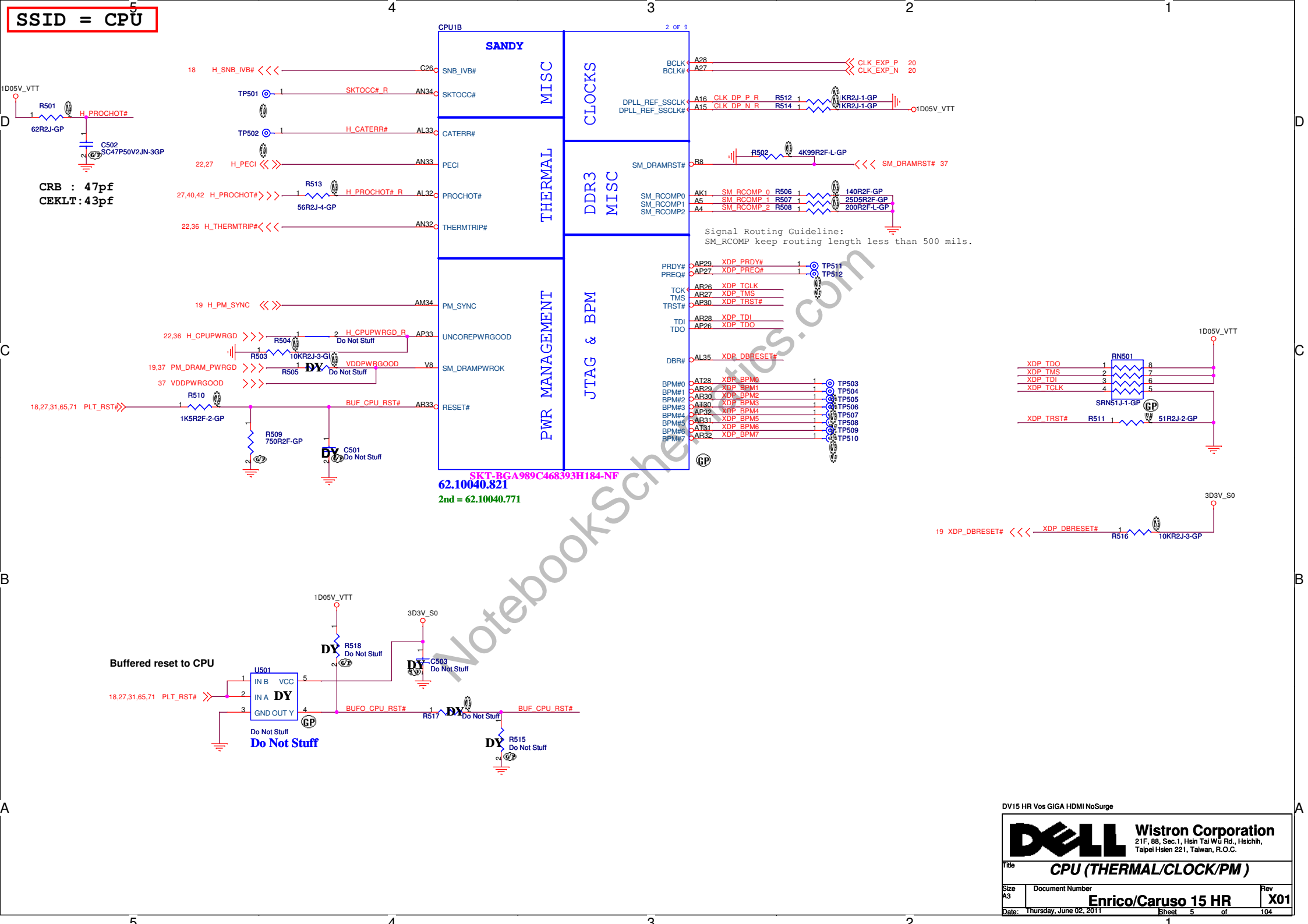
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Title: **CPU (PCIE/DMI/FDI)**

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SSID = CPU



CRB : 47pf
CEKLT : 43pf

Signal Routing Guideline:
SM_RCAMP keep routing length less than 500 mils.

SKT-BGA989C468393H184-NF
62.10040.821
2nd = 62.10040.771

Buffered reset to CPU

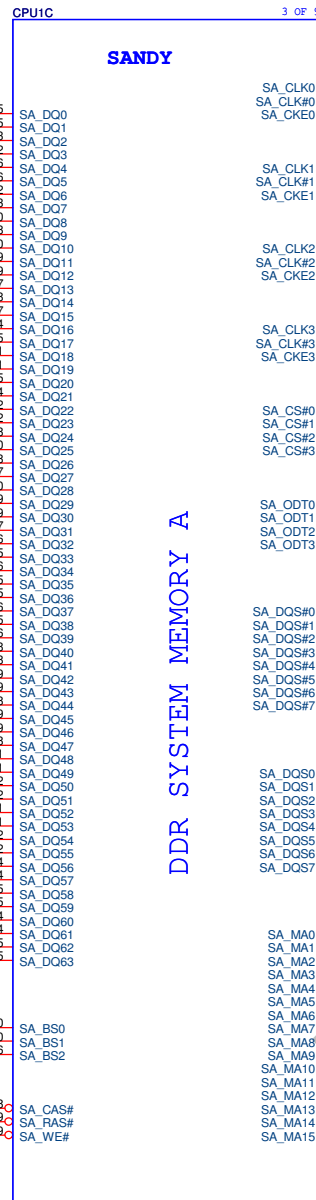
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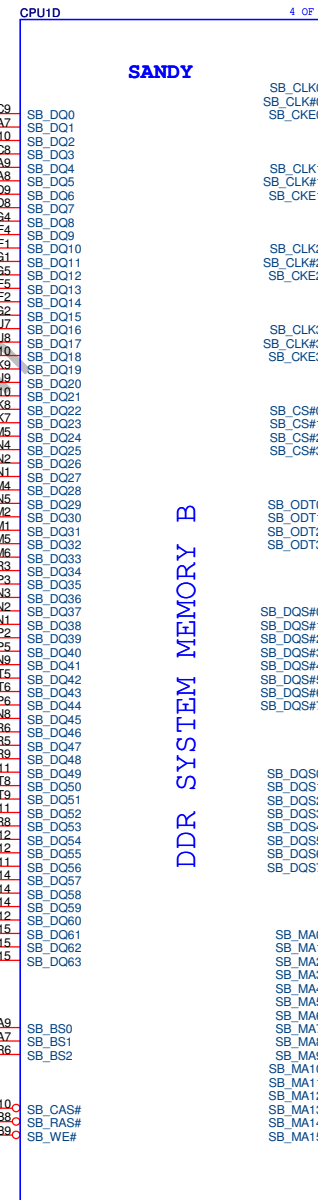
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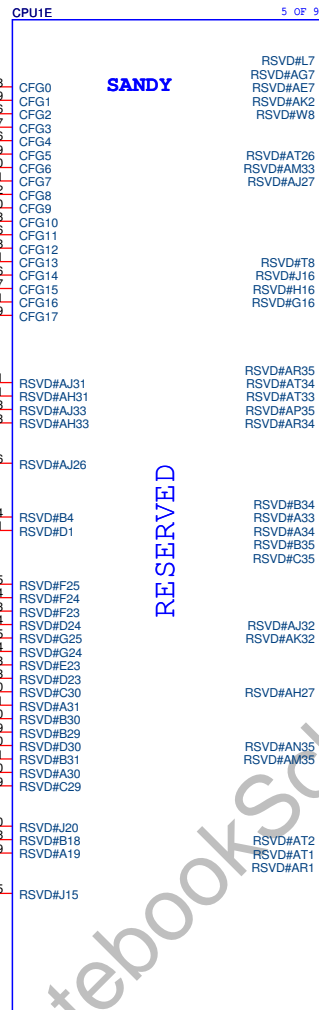
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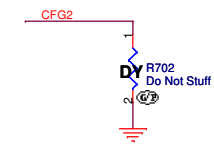
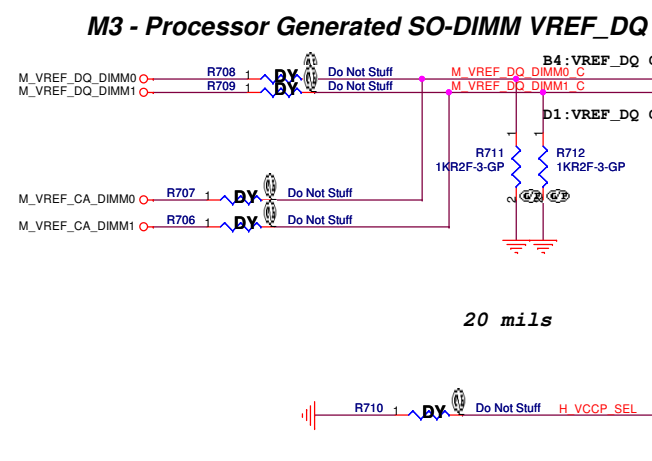


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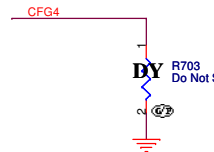
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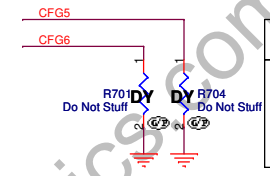
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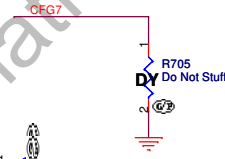
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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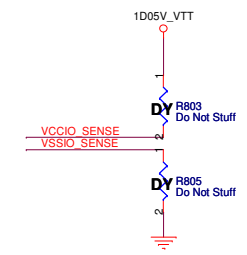
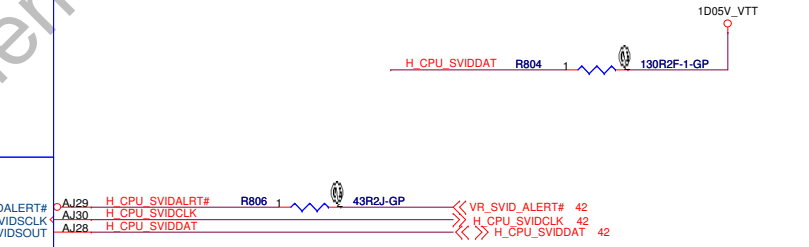
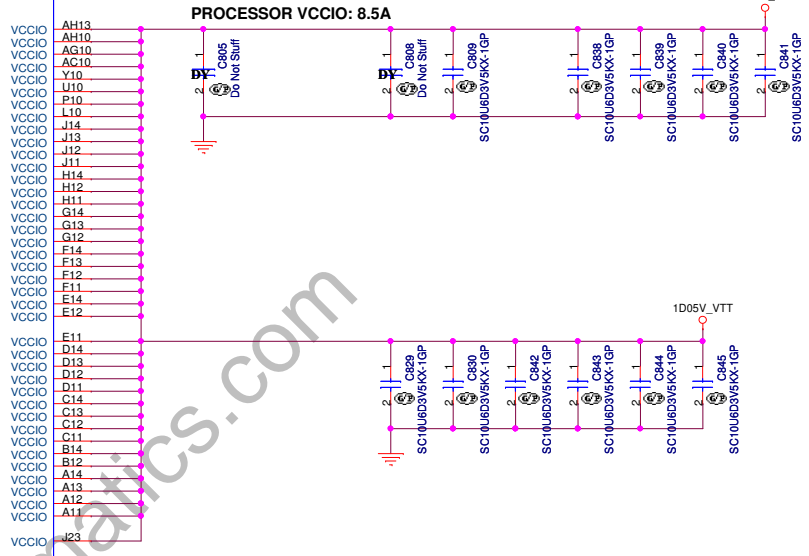
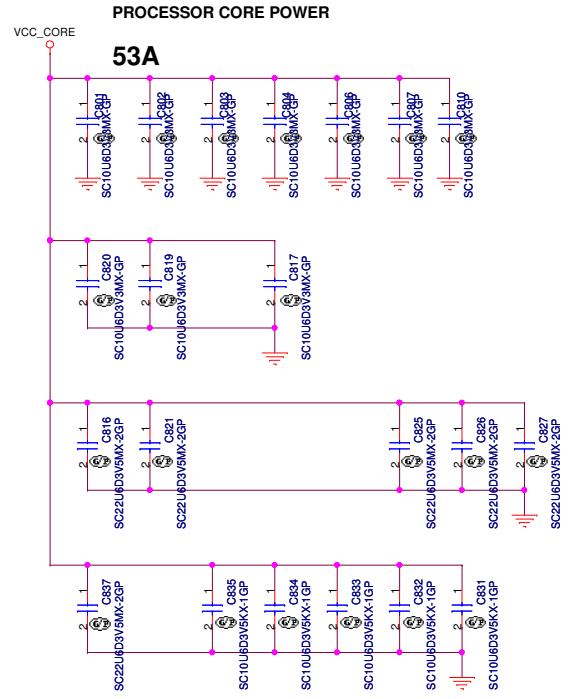
PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AG25 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
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- P26 VCC



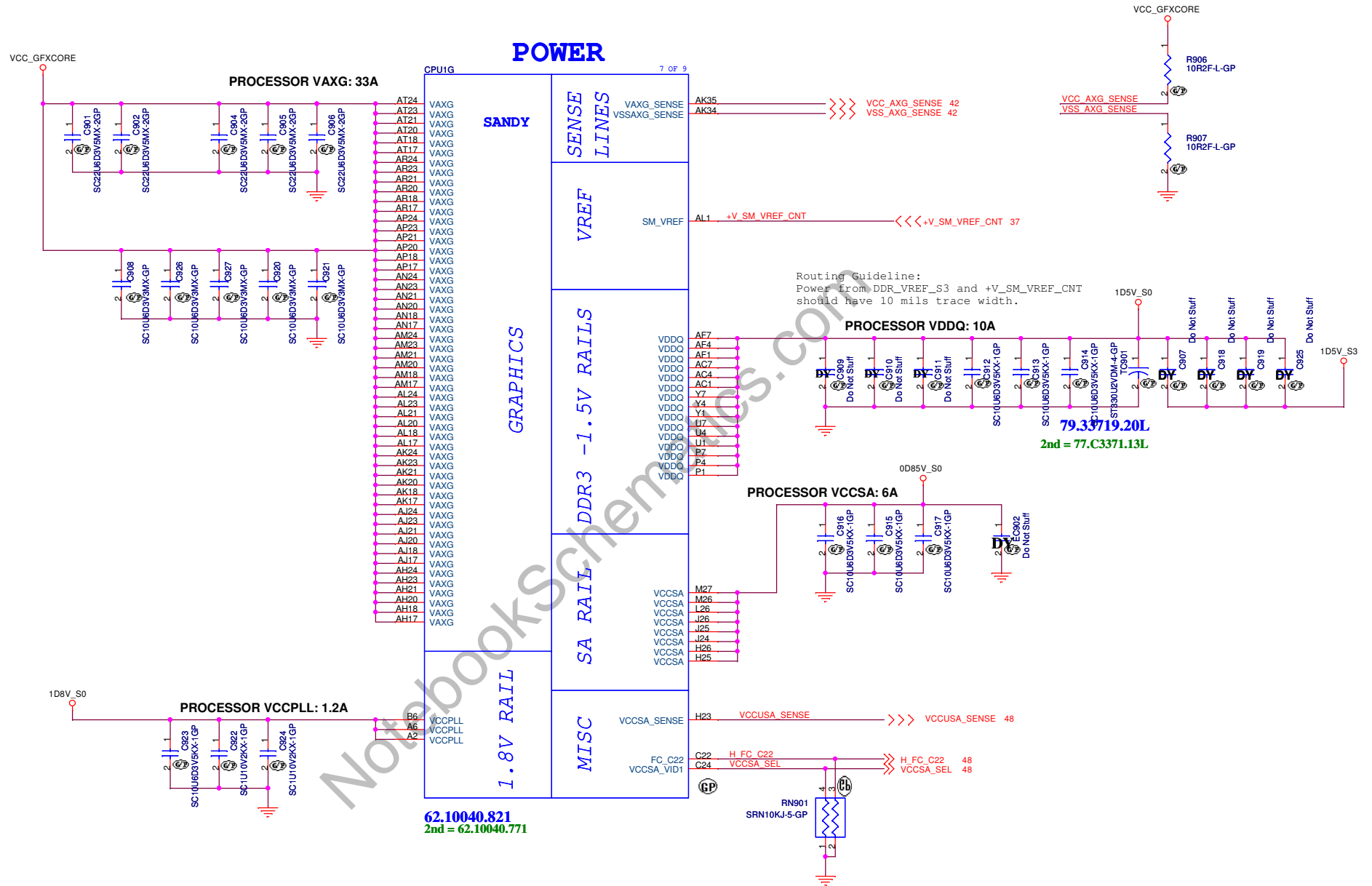
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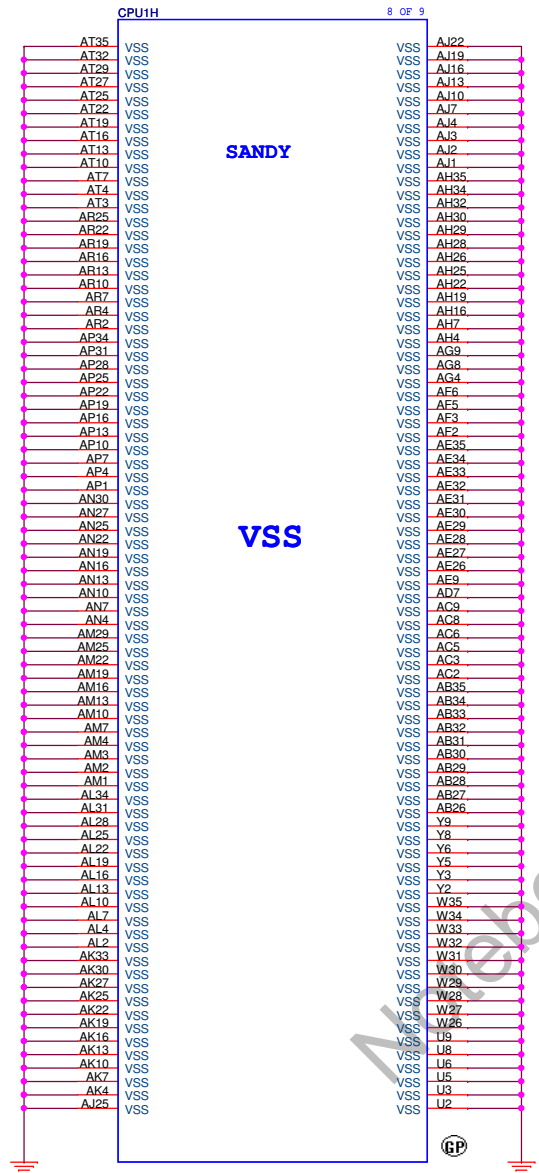
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Taipei Hsien 221, Taiwan, R.O.C.

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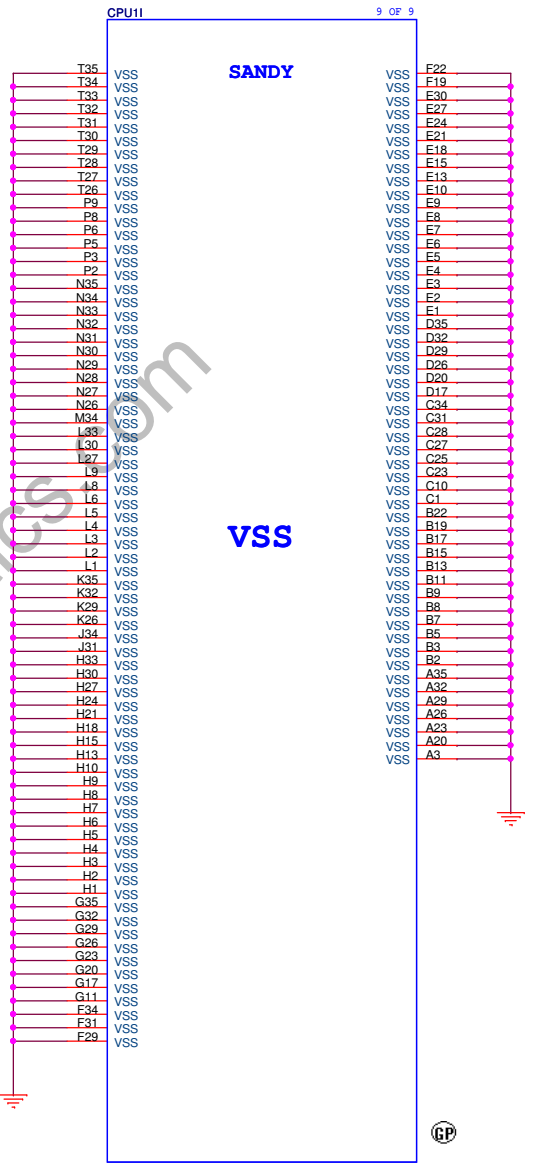
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SSID = CPU



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62.10040.821
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Title: **CPU (VSS)**

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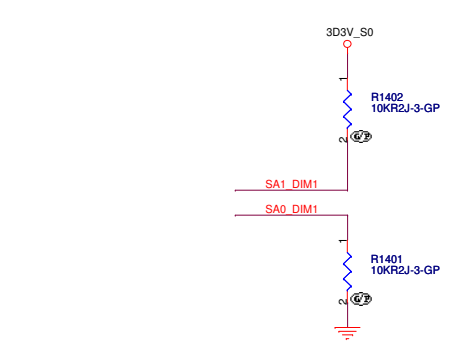
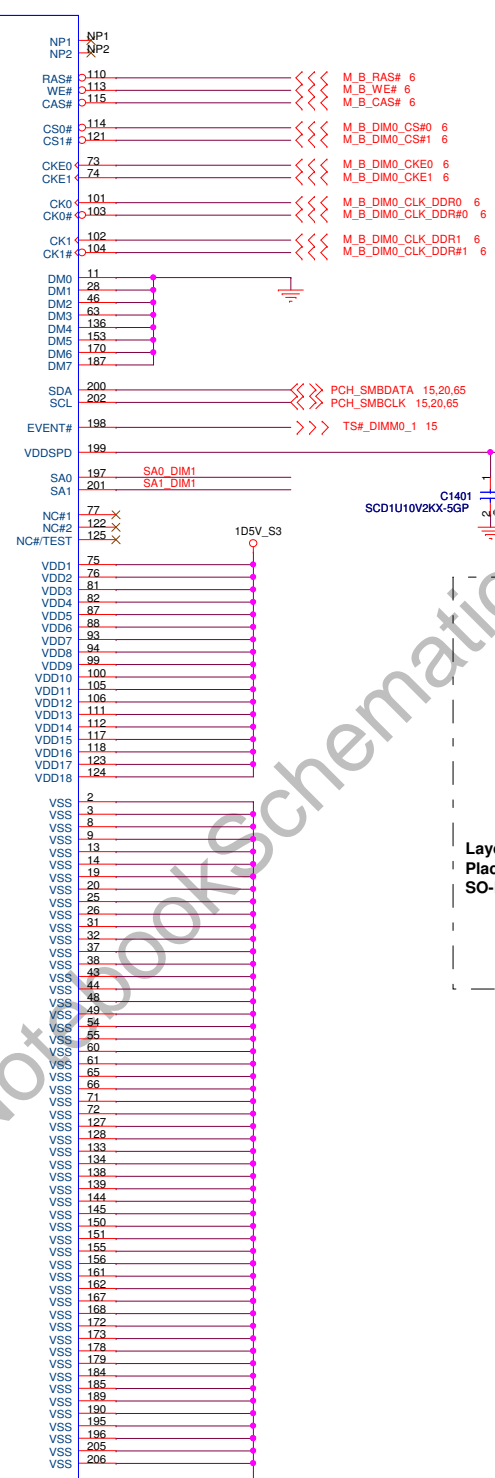
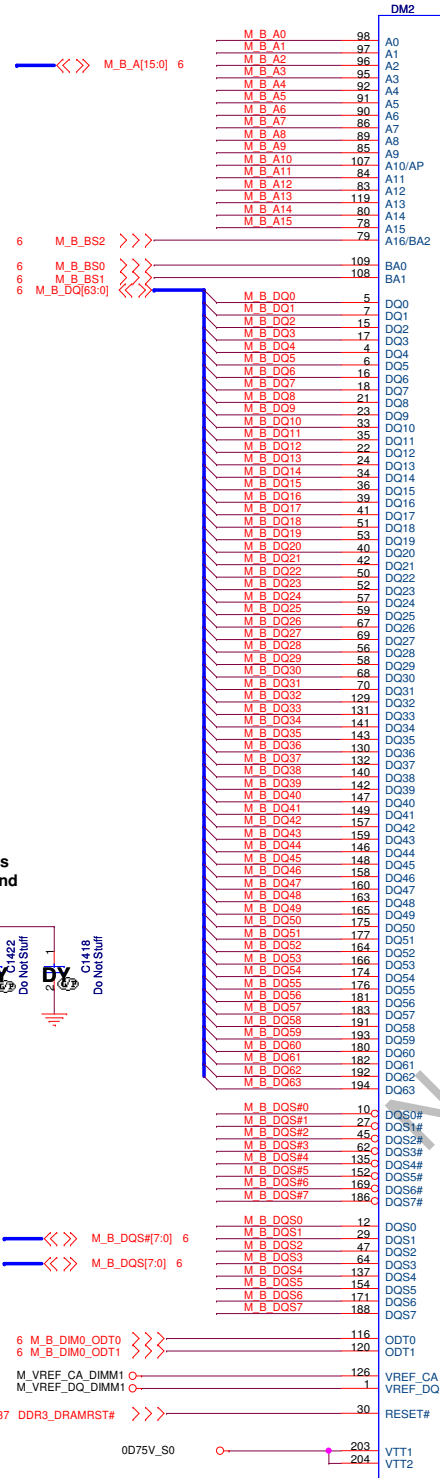
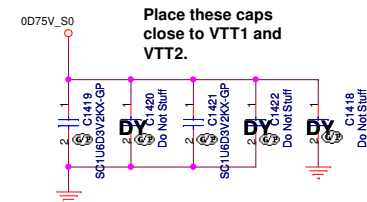
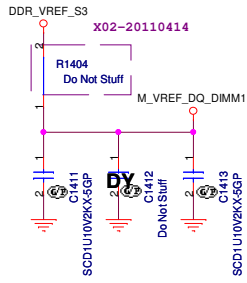
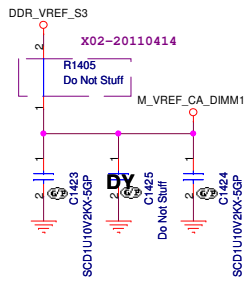
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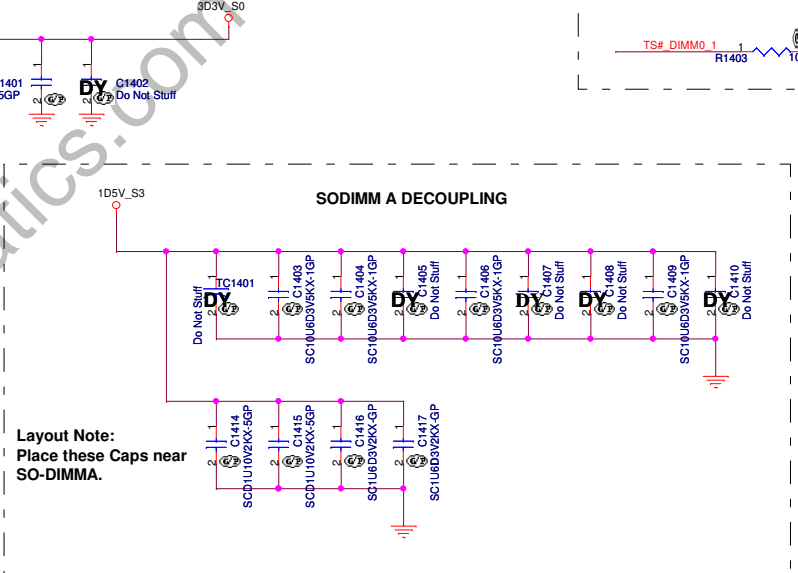
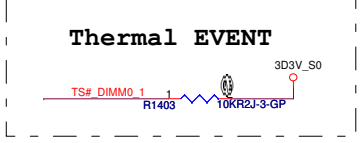
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Reserved		
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SSID = MEMORY



Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30

 If SA0_DIM0 = 0, SA1_DIM0 = 1
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32



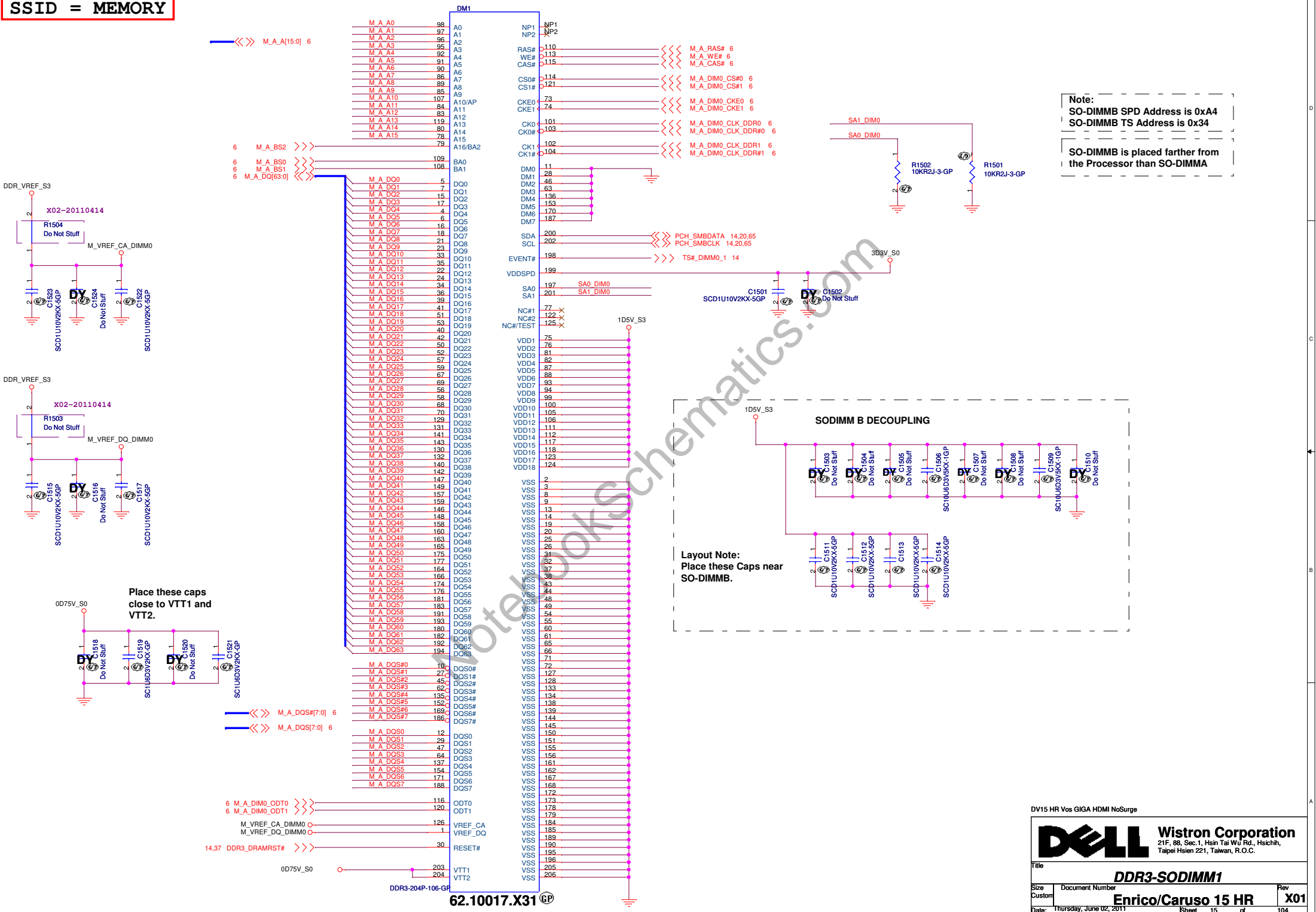
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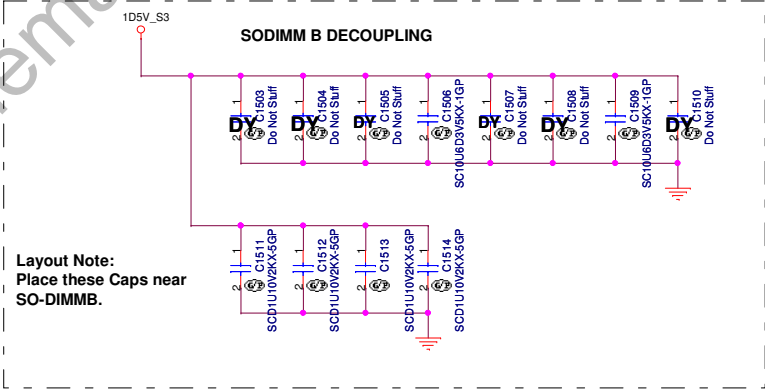


Title DDR3-SODIMM2		
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SSID = MEMORY



Note:
 SO-DIMM SPD Address is 0xA4
 SO-DIMM TS Address is 0x34
 SO-DIMM is placed farther from the Processor than SO-DIMMA



Layout Note:
 Place these Caps near SO-DIMM.

Place these caps close to VTT1 and VTT2.

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Title: **DDR3-SODIMM1**

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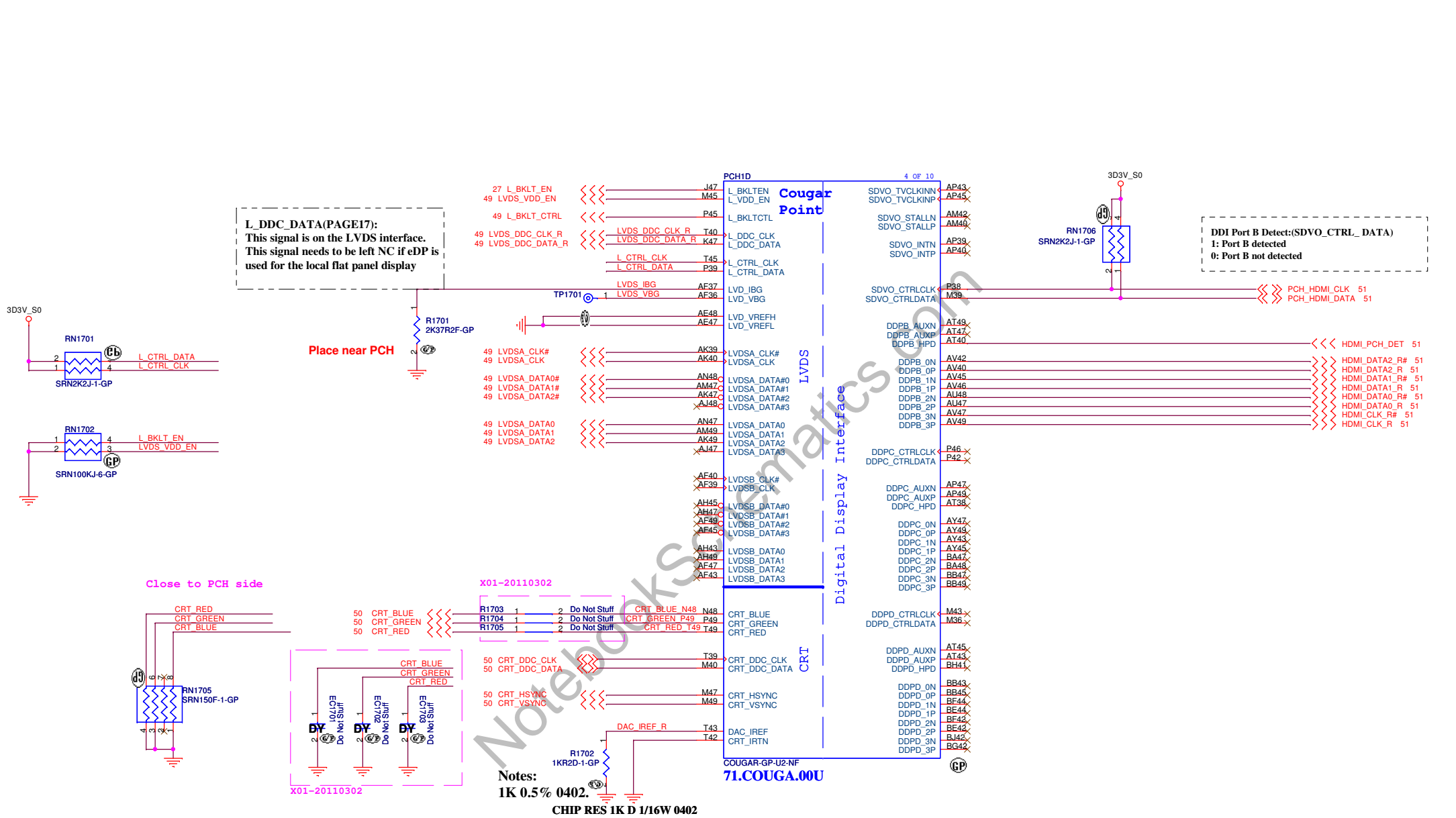
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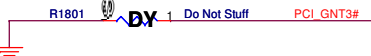
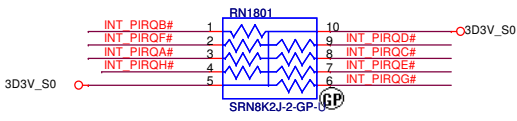
DV15 HR Vos GIGA HDMI NoSurge



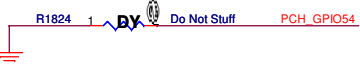
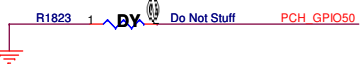
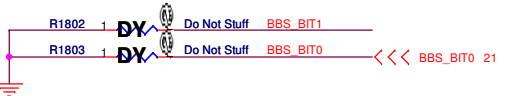
Title		
Reserved		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
Date: Thursday, June 02, 2011	Sheet 16	of 104



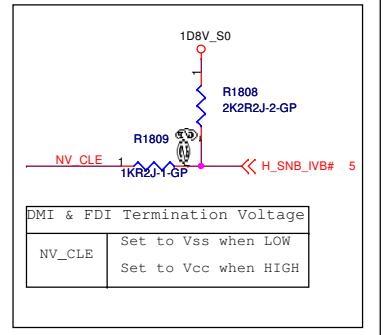
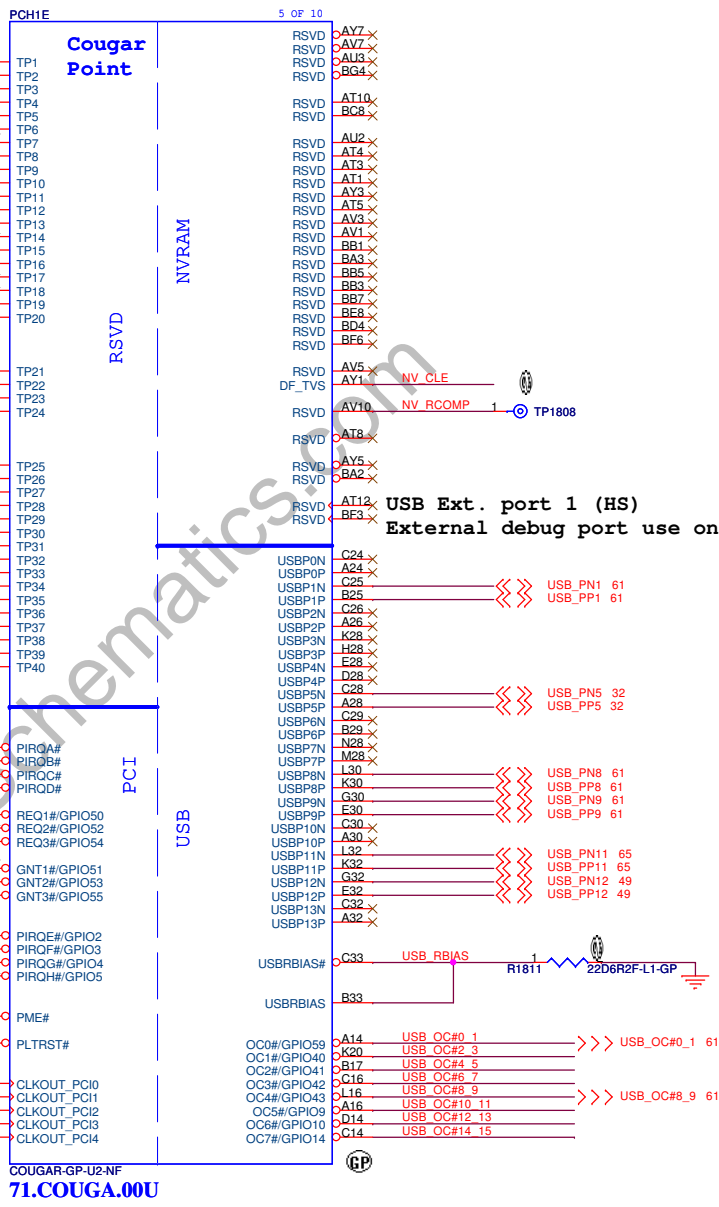
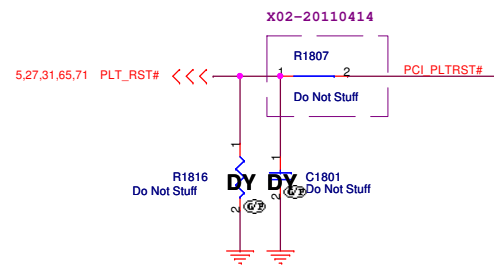
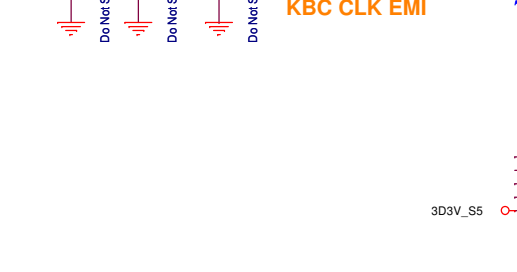
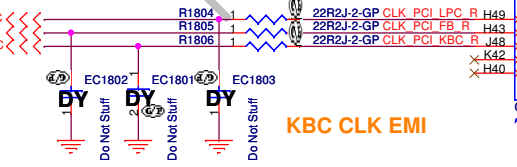
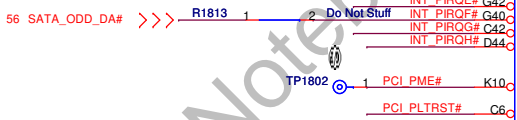
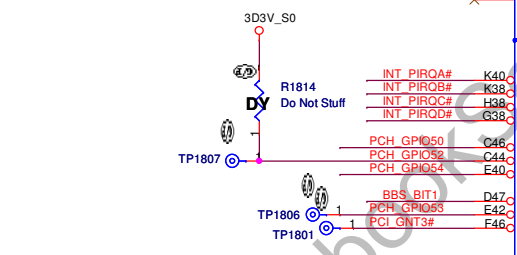
SSID = PCH



Al6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW
	Set to Vcc when HIGH

USB Ext. port 1 (HS)
External debug port use on Huron river platform
USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

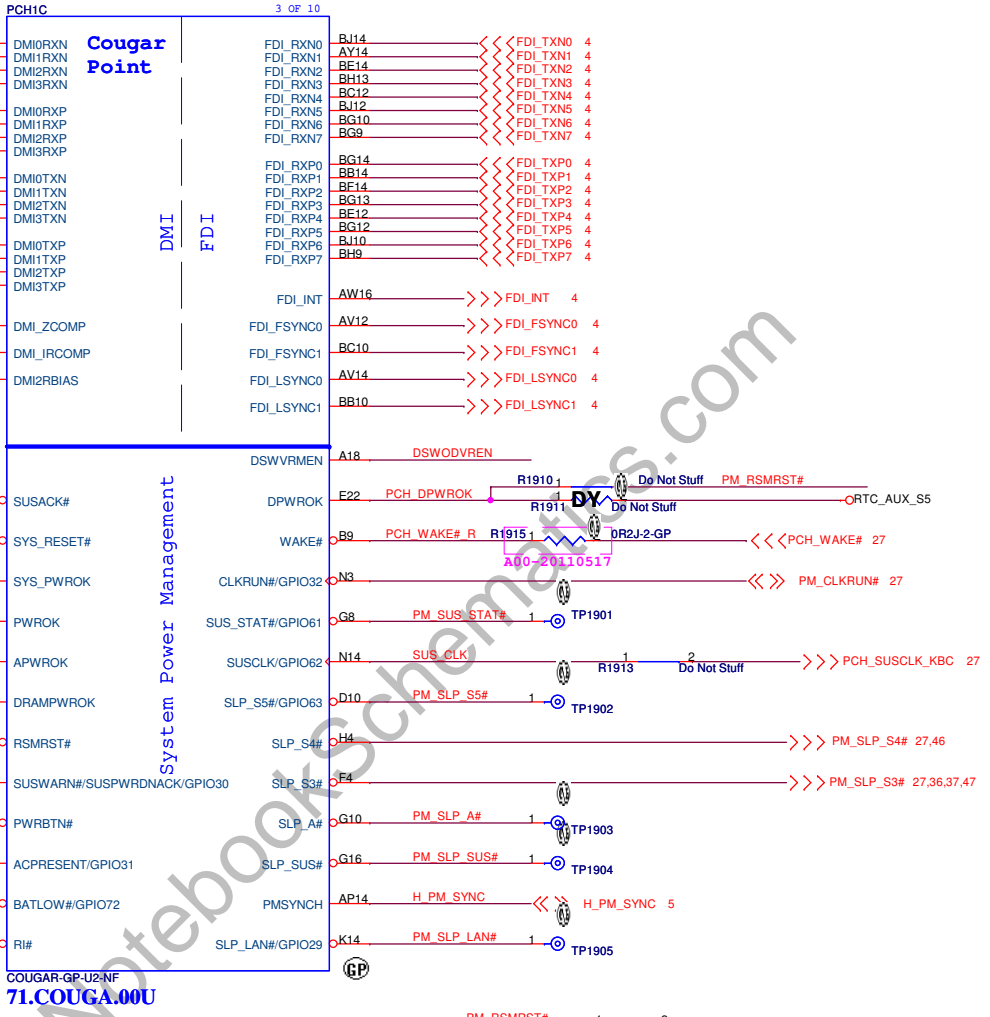
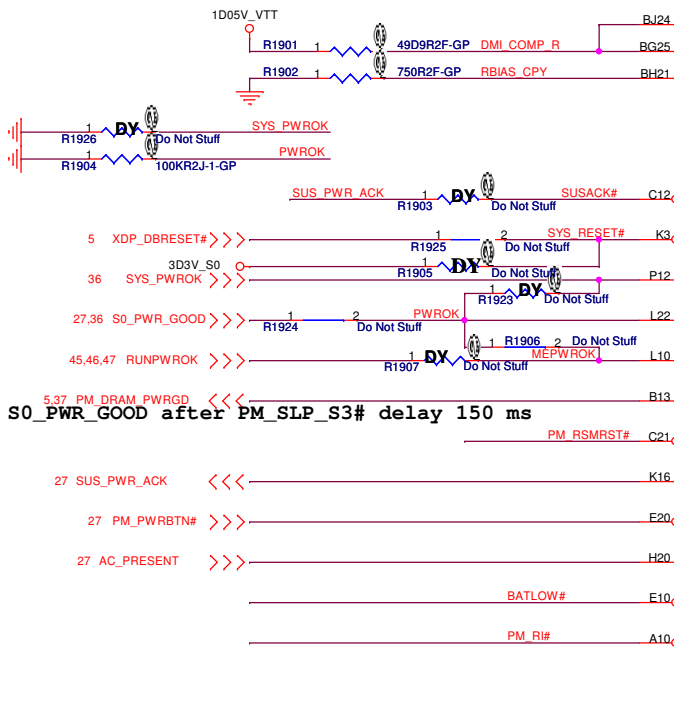
Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

PCH (PCI/USB/NVRAM)
 Title: Enrico/Carus 15 HR
 Size A3 Document Number Rev
 Date: Thursday, June 02, 2011 Sheet 18 of 104

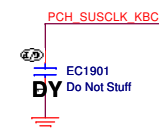
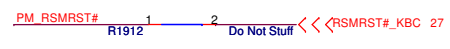
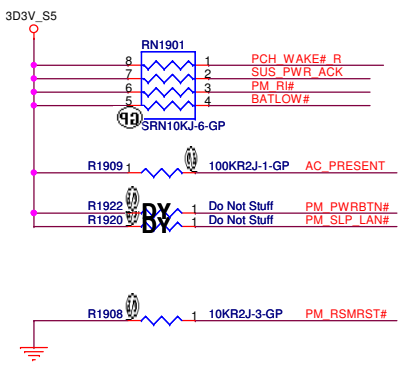
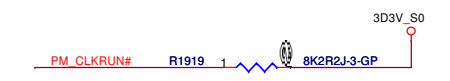
SSID = PCH



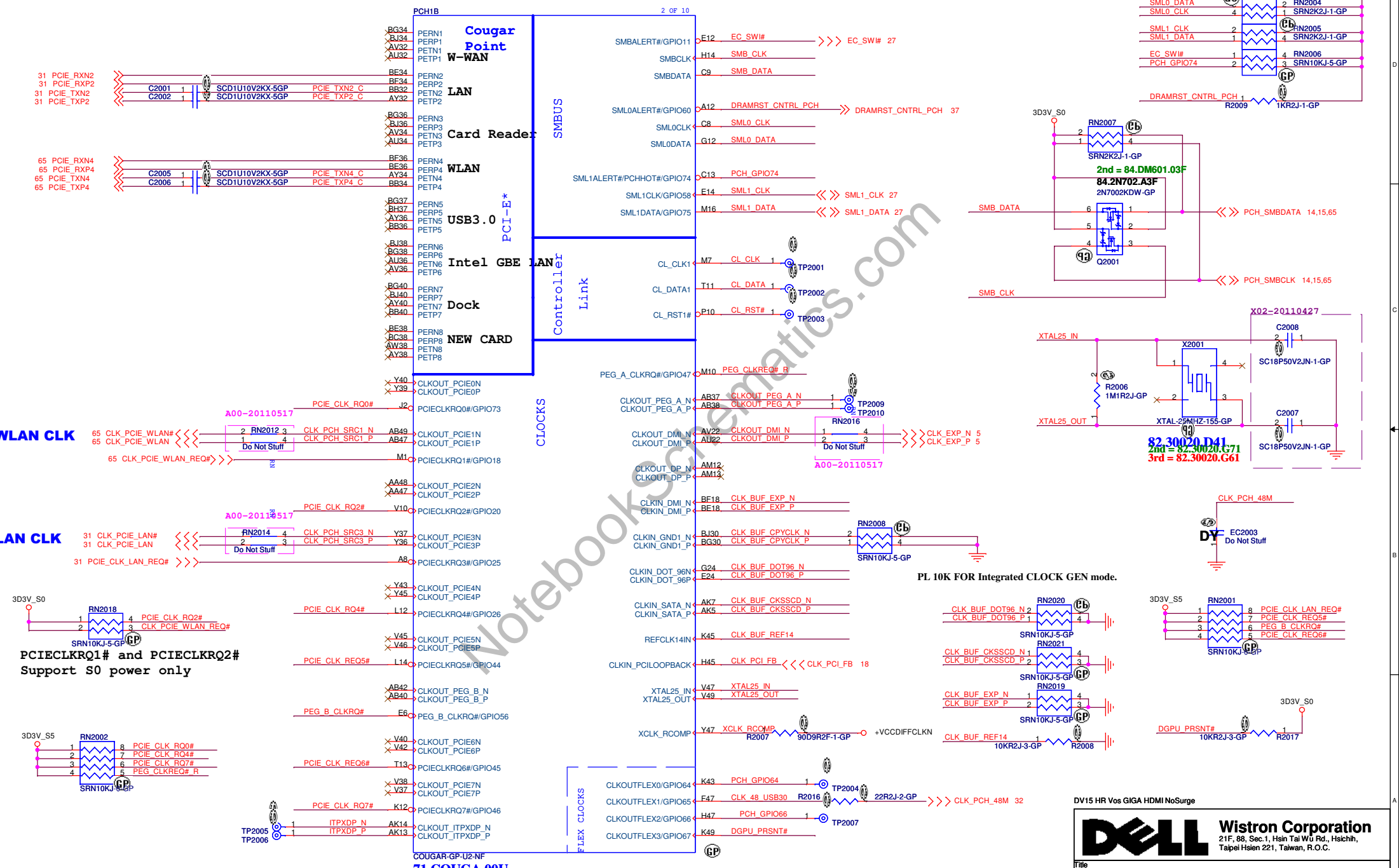
Signal Routing Guideline:
 DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
 DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



SSID = PCH



- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
 - Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
 if more than 2 PCI clocks + PCI loopback are routed.

DV15 HR Vos GIGA HDMI NoSurge

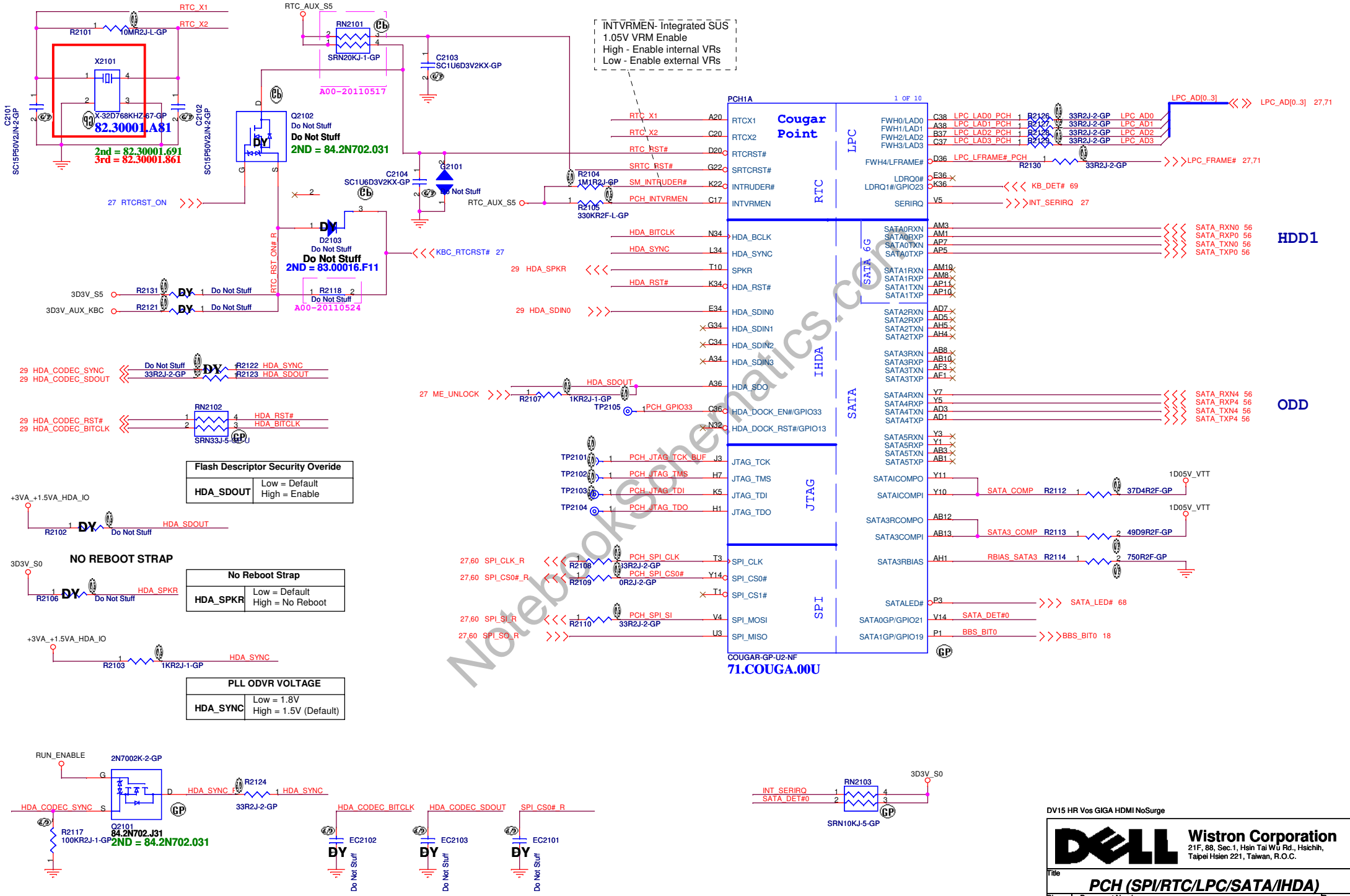
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

Date: Thursday, June 02, 2011 Sheet 20 of 104

SSID = PCH



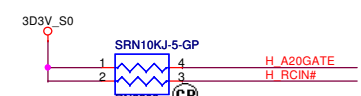
DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

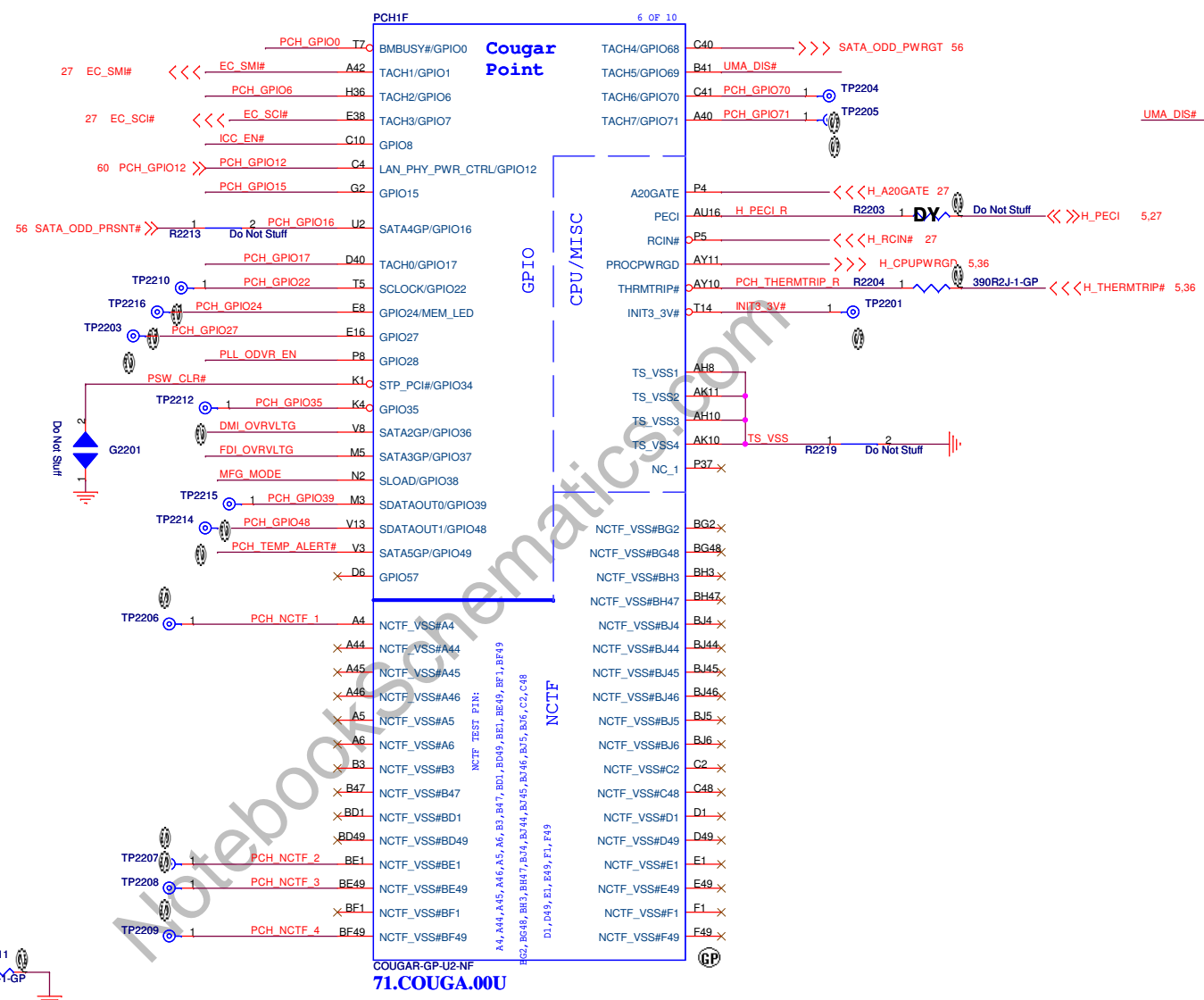
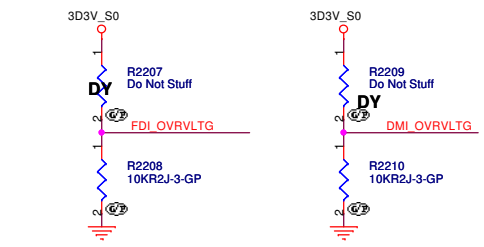
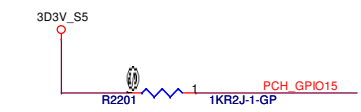
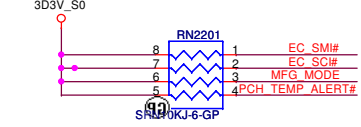
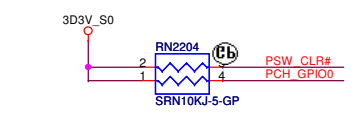
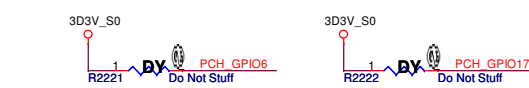
Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

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SSID = PCH

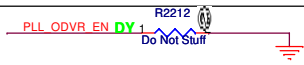


GPIO27 has a weak[20K] internal pull up. To enable on-die PLL Voltage regulator, should not place external pull down.



PLL ON DIE VR ENABLE

NOTE: This signal has a weak internal pull-up 20k
 ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
 DISABLED -- LOW (R2212 STUFFED)



DW15 HR Vos GIGA HDMI NoSurge

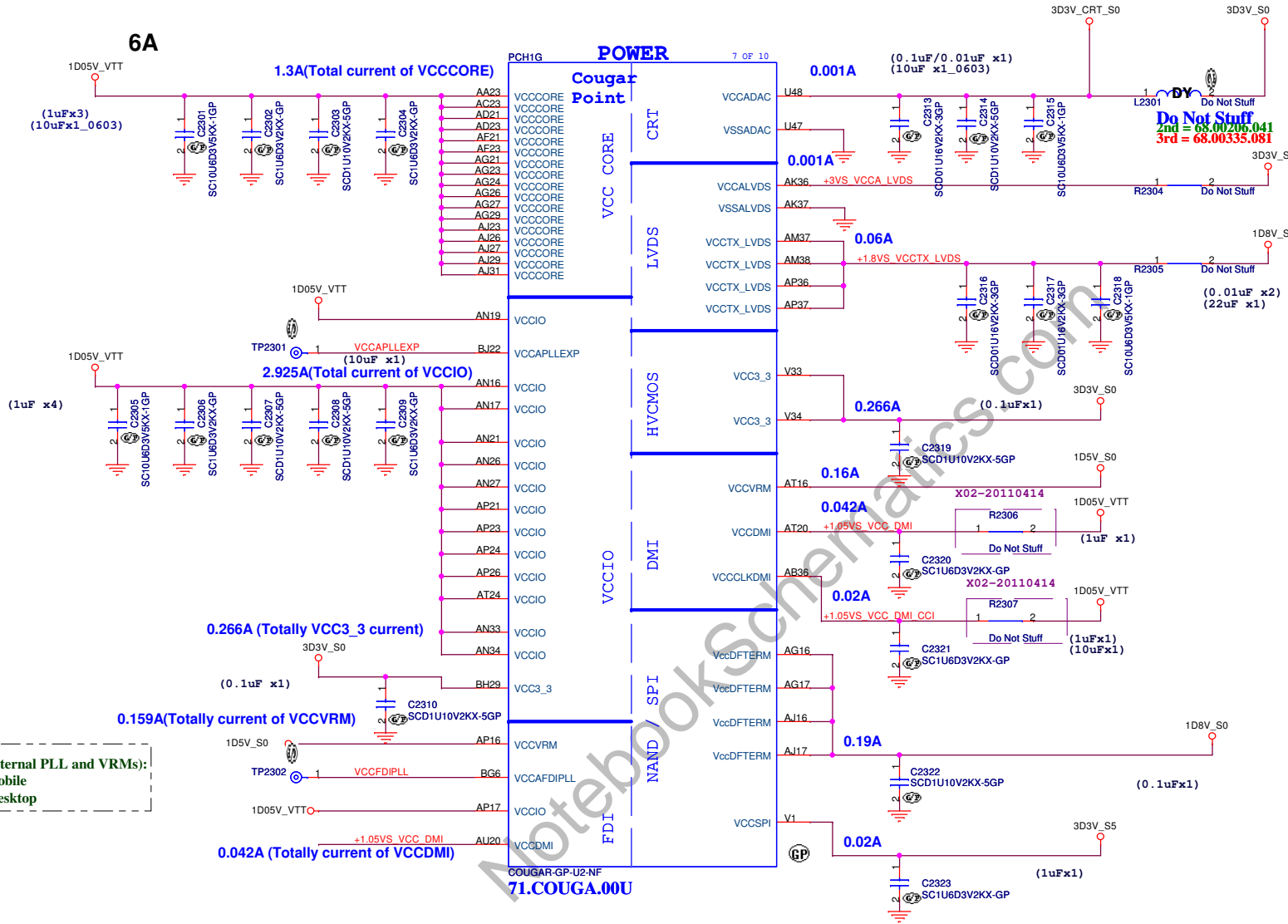
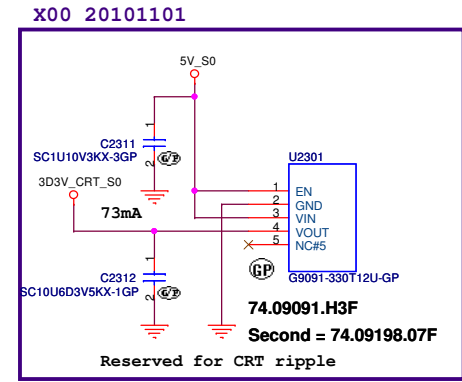
Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

Size A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

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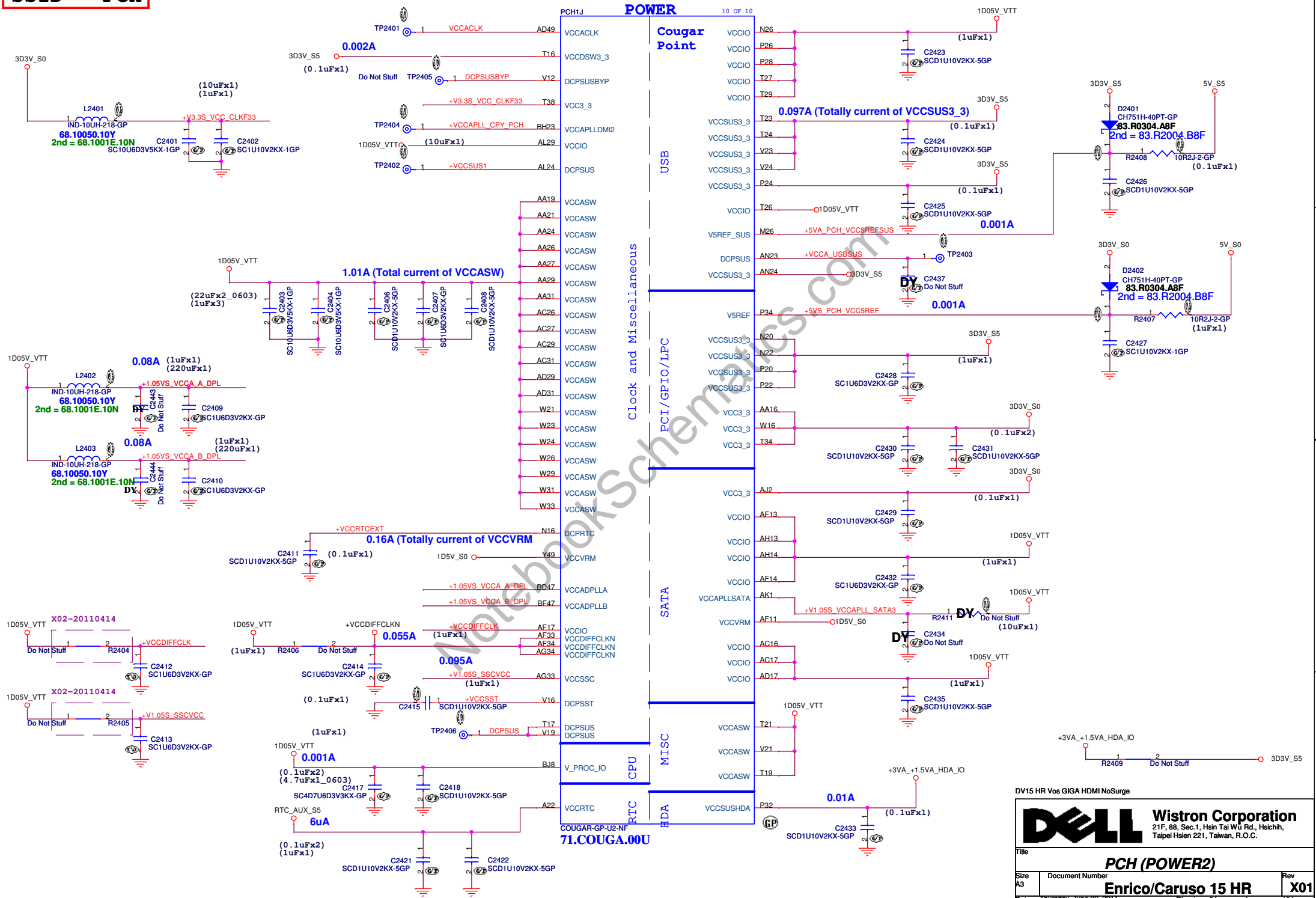
SSID = PCH



VCCVRM (Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop

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SSID = PCH



POWER

Cougar Point

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

PCH1J 10 OF 10

71.COUGA.000

DV15 HR Vos GIGA HDMI NoSurge

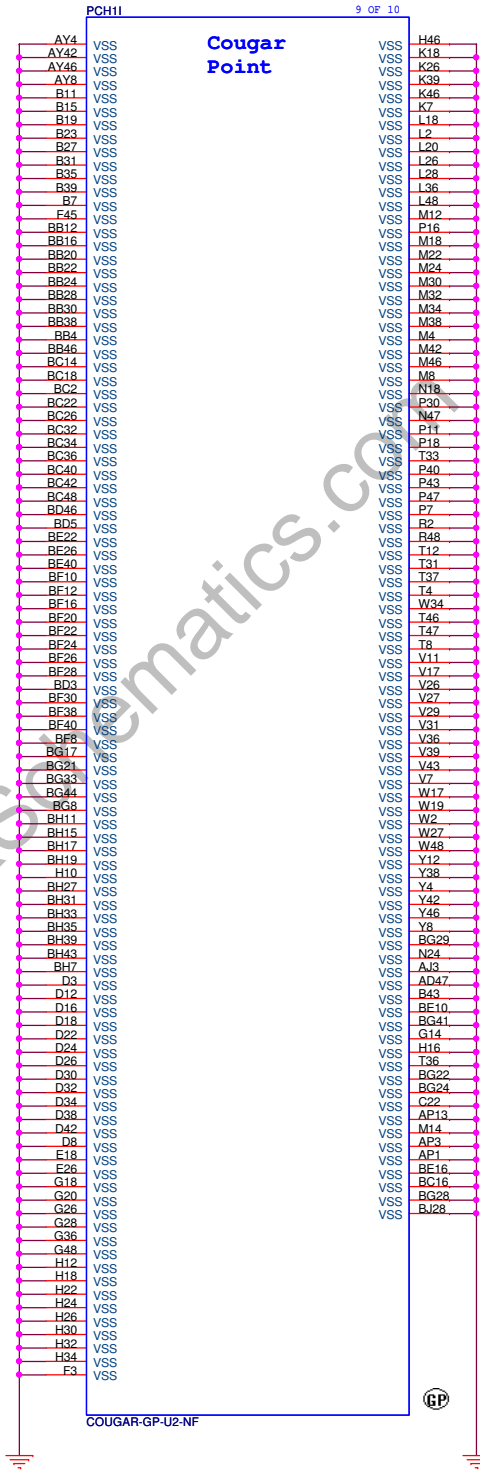
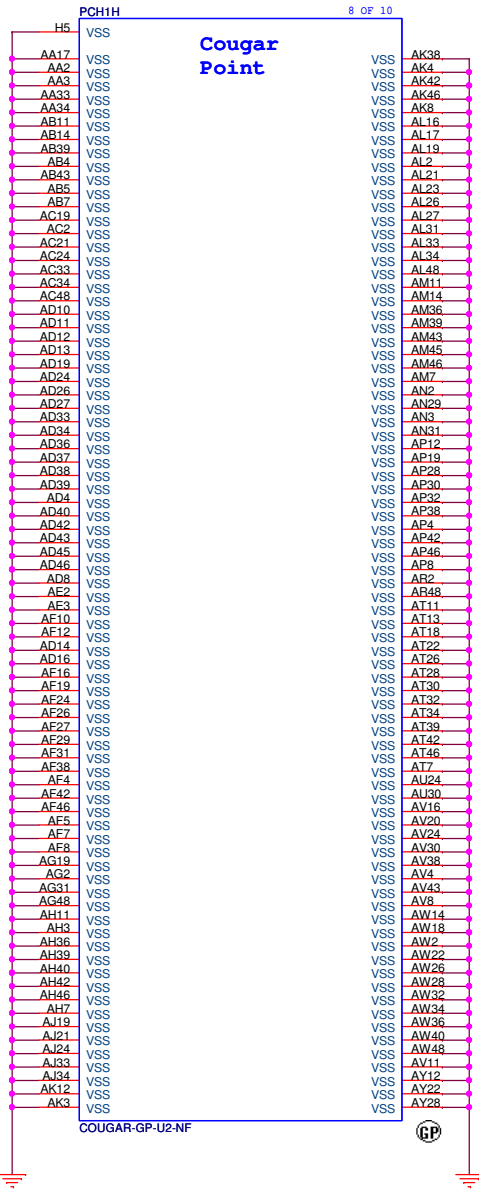
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER2)**

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Date: Thursday, June 02, 2011	Enrico/Carus 15 HR	X01

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SSID = PCH



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Title		
PCH (VSS)		
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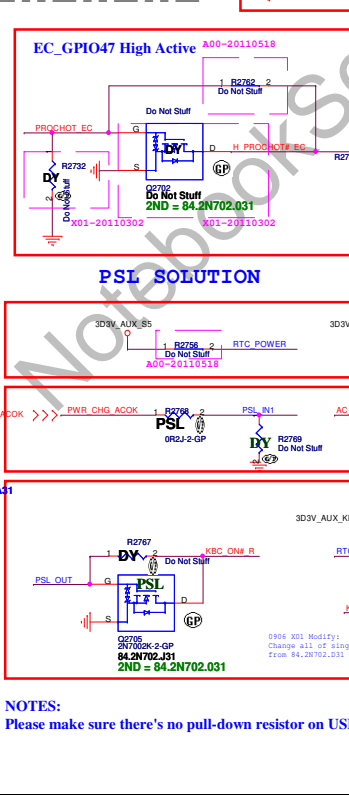
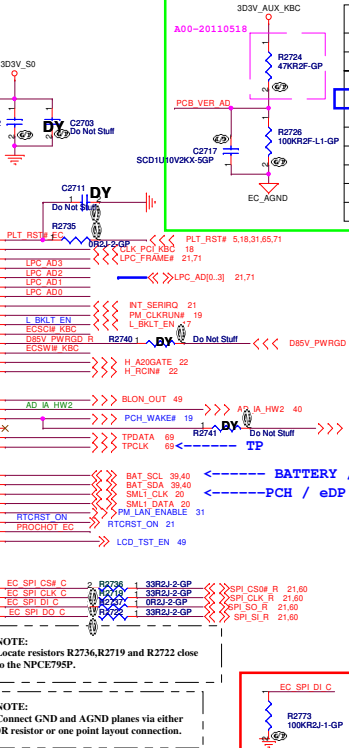
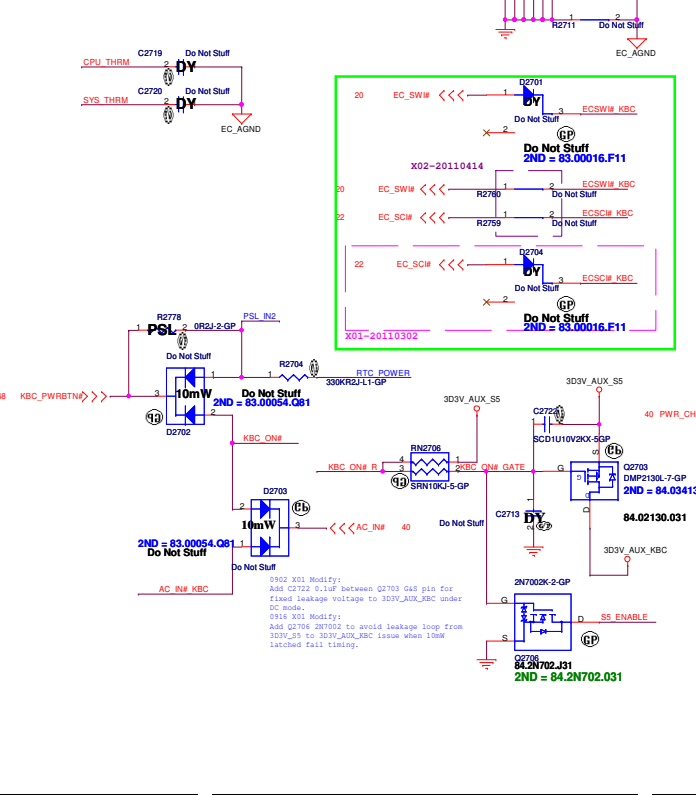
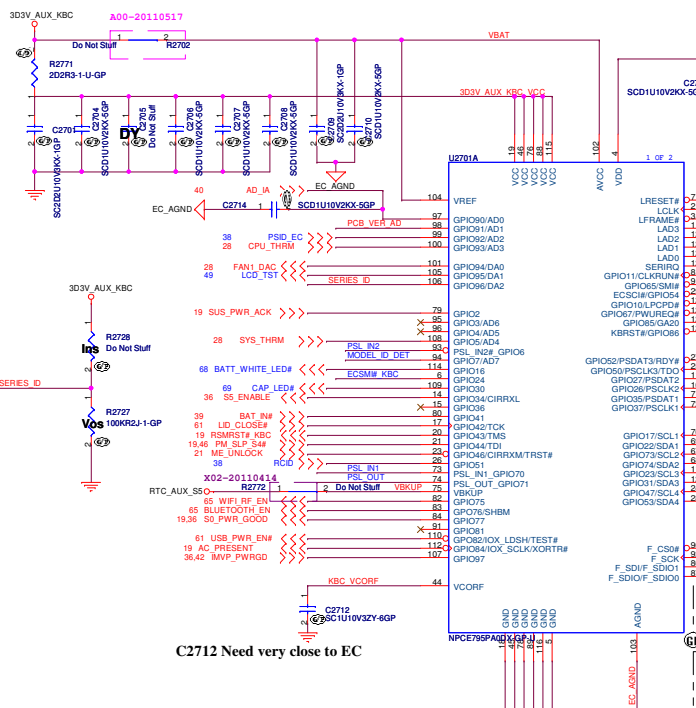
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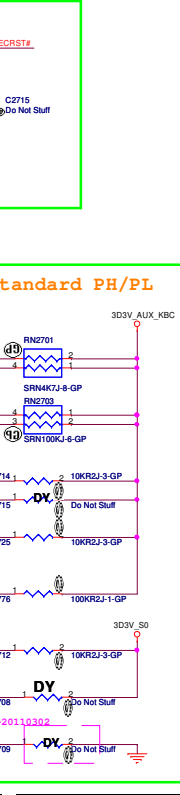
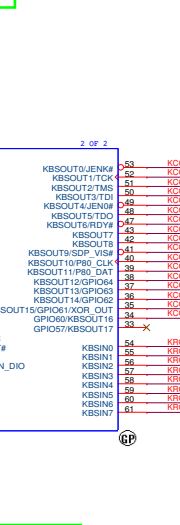
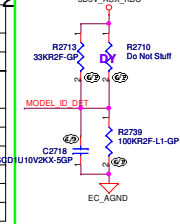
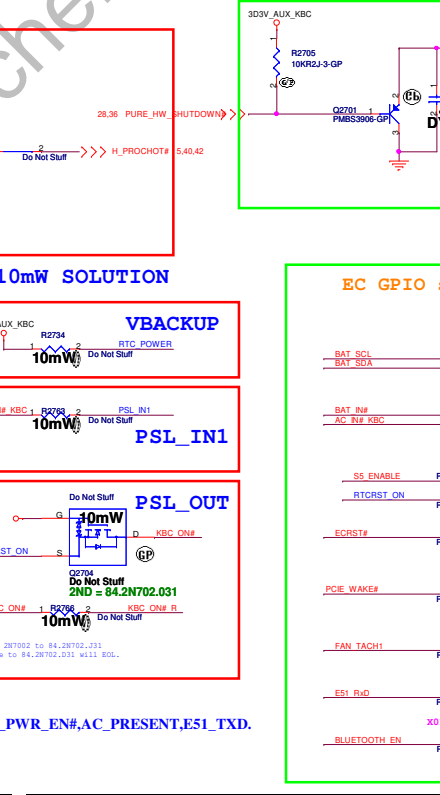
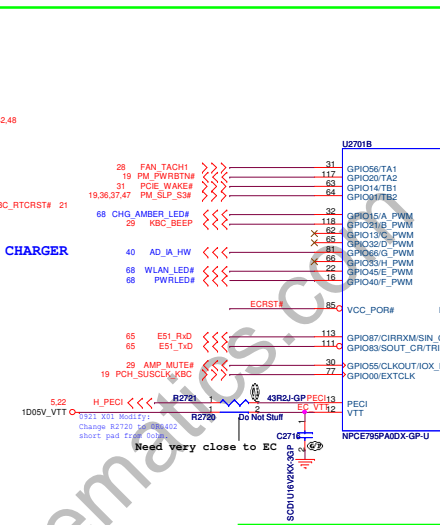
DV15 HR Vos GIGA HDMI NoSurge

	Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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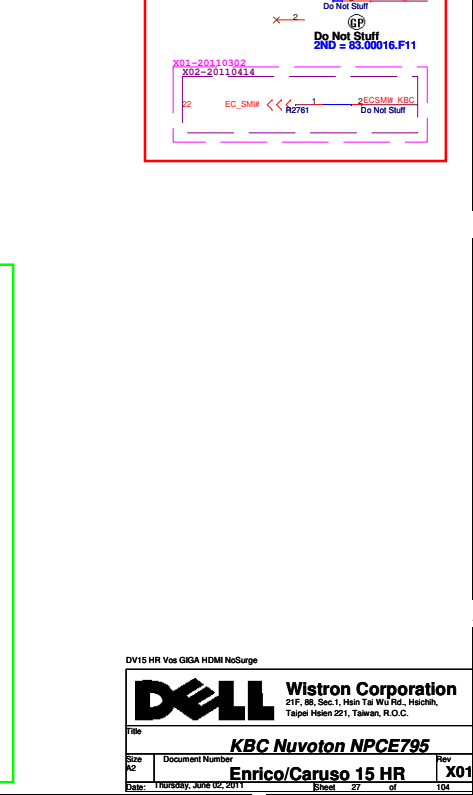
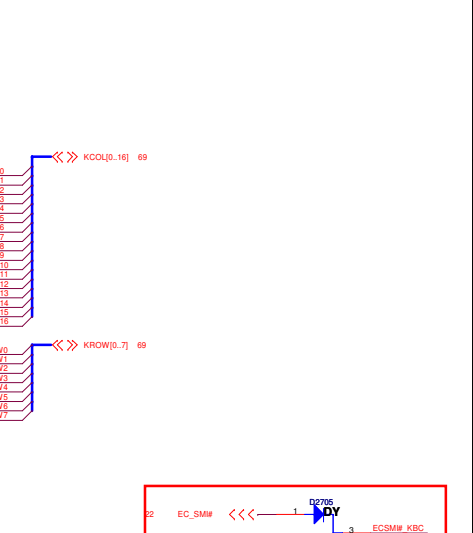
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PCB VERSION A(D/PIN#8)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.388V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V



MODEL_ID_DET(GPIO#7)	FULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_UMA	100.0K	10.0K(64.10025.GDL)	3.0V
DV14_DIS_PX	100.0K	20.0K(64.20025.GDL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.GDL)	2.24V
Reserved	100.0K	64.9K(64.64925.GDL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.388V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V



NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,ES1_TXD.

DIV15 HR Vos GIGA HDMI NoSurge

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 301, Taiwan, R.O.C.

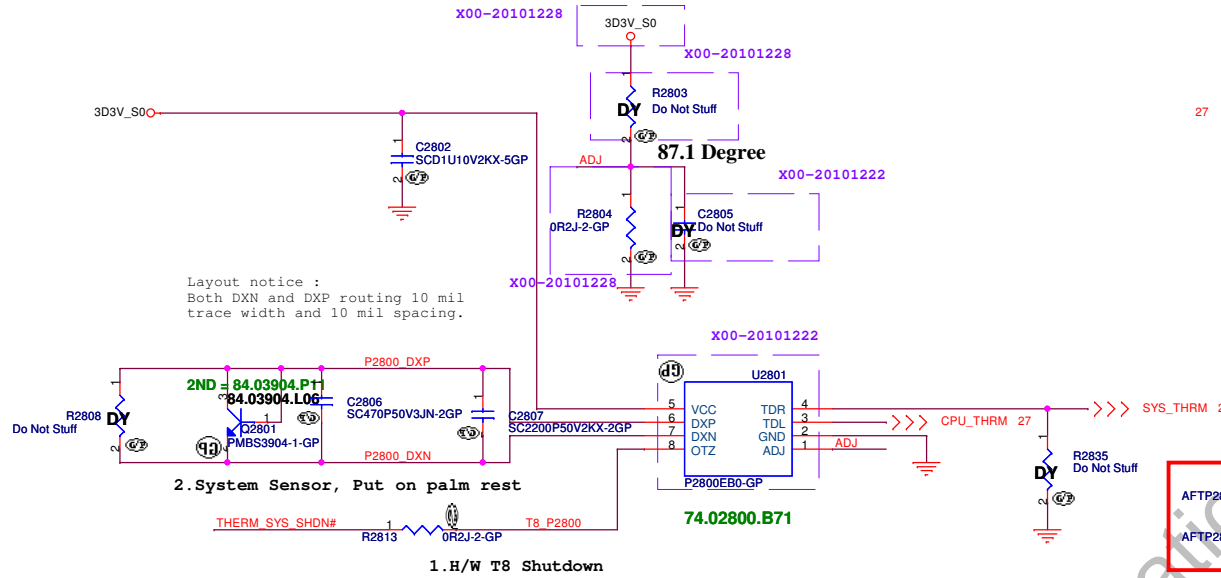
File: **KBC NuvoTon NPCE795**
Rev: **X01**

Size: **Document Number**
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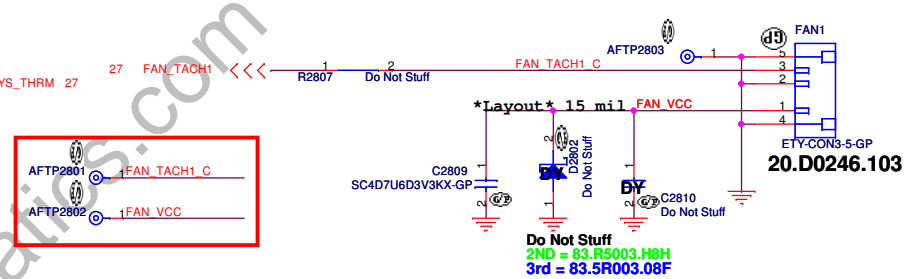
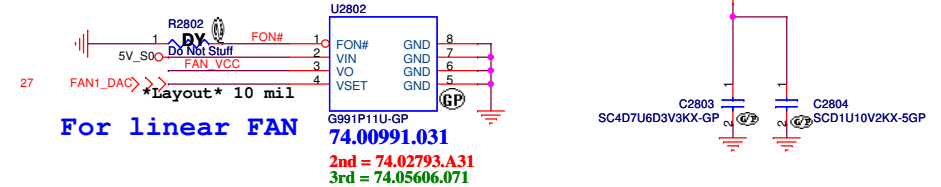
Date: **Thursday, June 16, 2011** Sheet **27** of **104**

SSID = Thermal

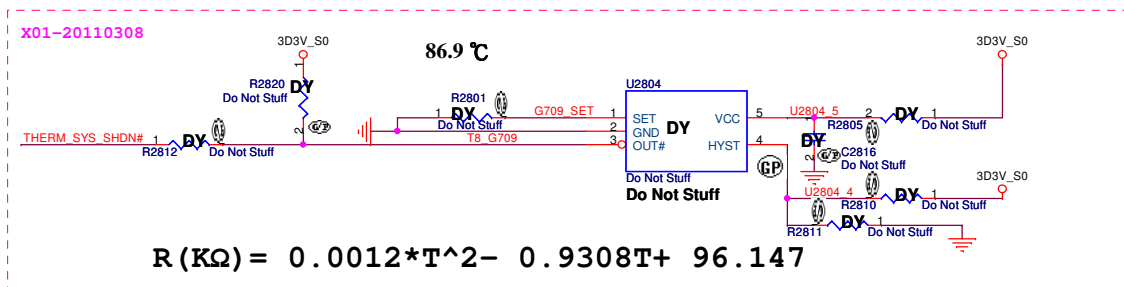
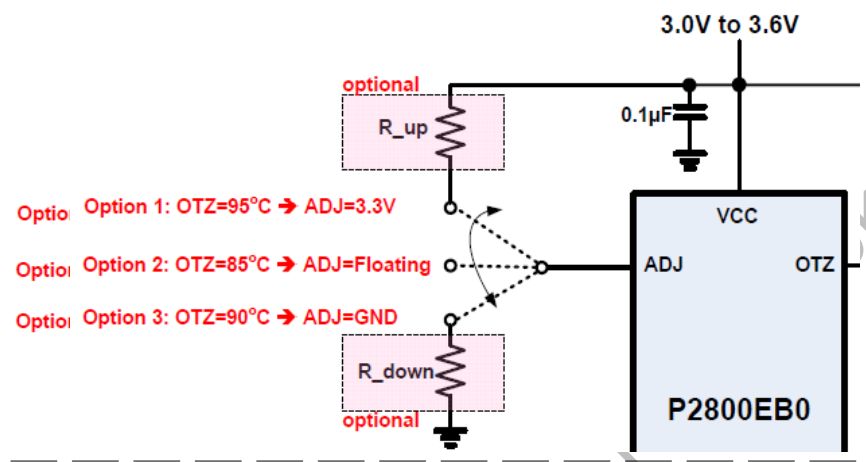
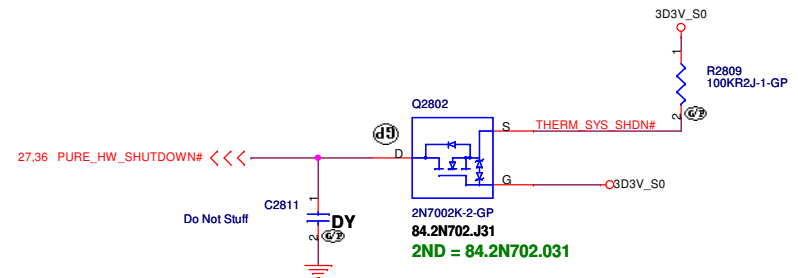
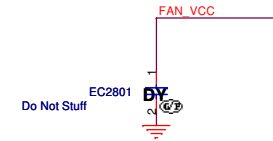
Thermal sensor P2800



Fan controller G991



EMI/ESD



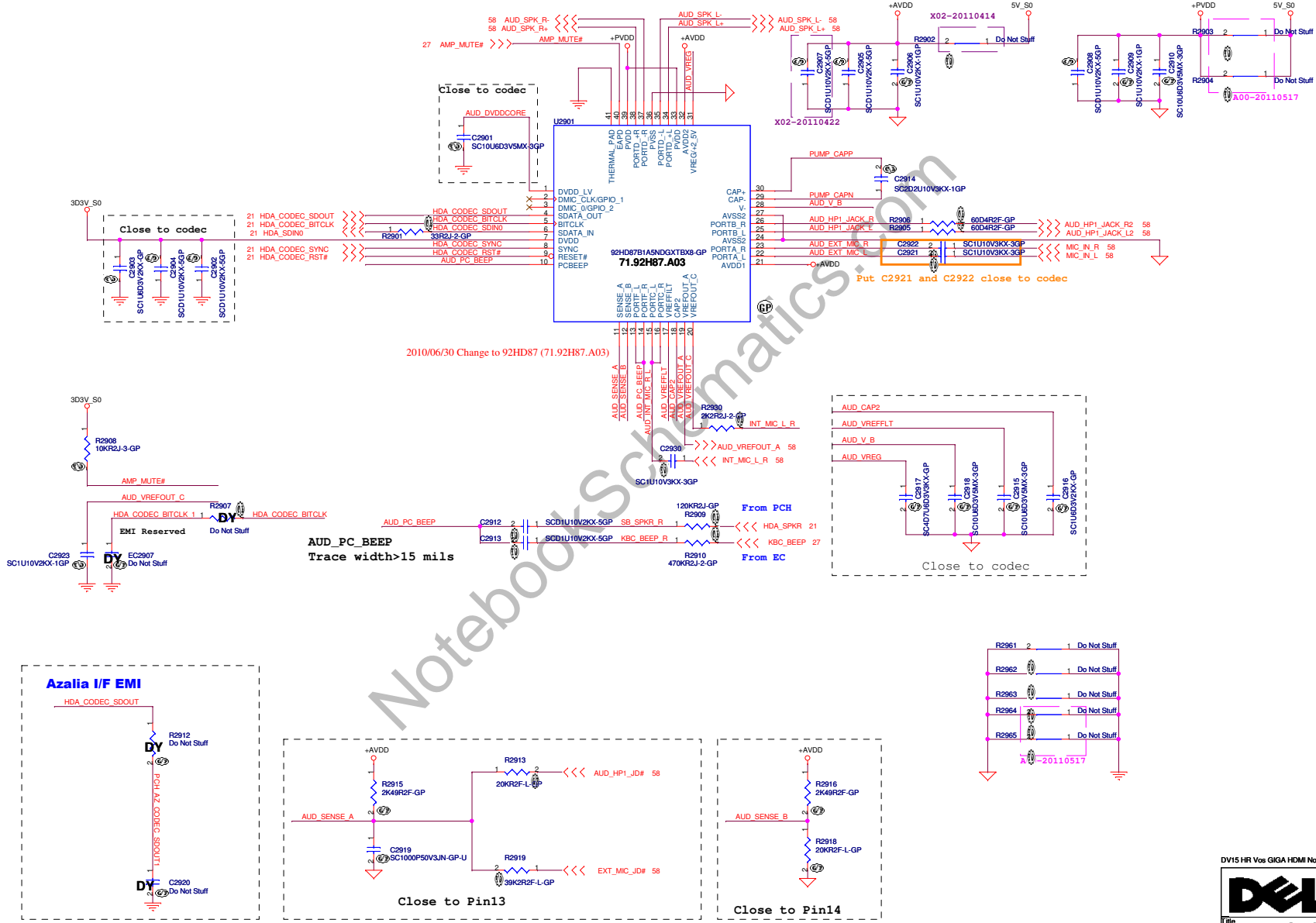
DV15 HR Vos GIGA HDMI NoSurge

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal P2800/Fan Controller P2793**

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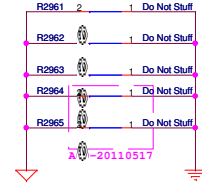
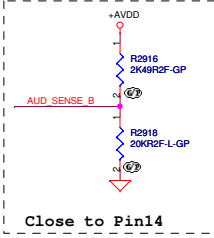
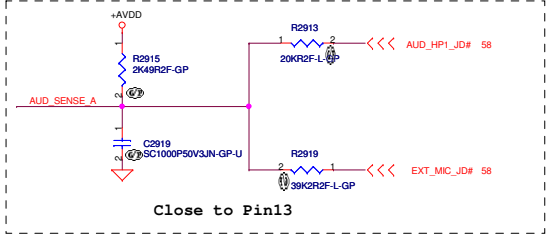
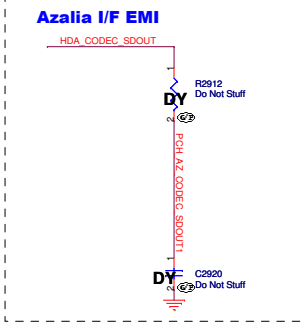
SSID = AUDIO



2010/06/30 Change to 92HD87 (71.92H87.A03)

Put C2921 and C2922 close to codec

AUD_PC_BEEP
Trace width > 15 mils



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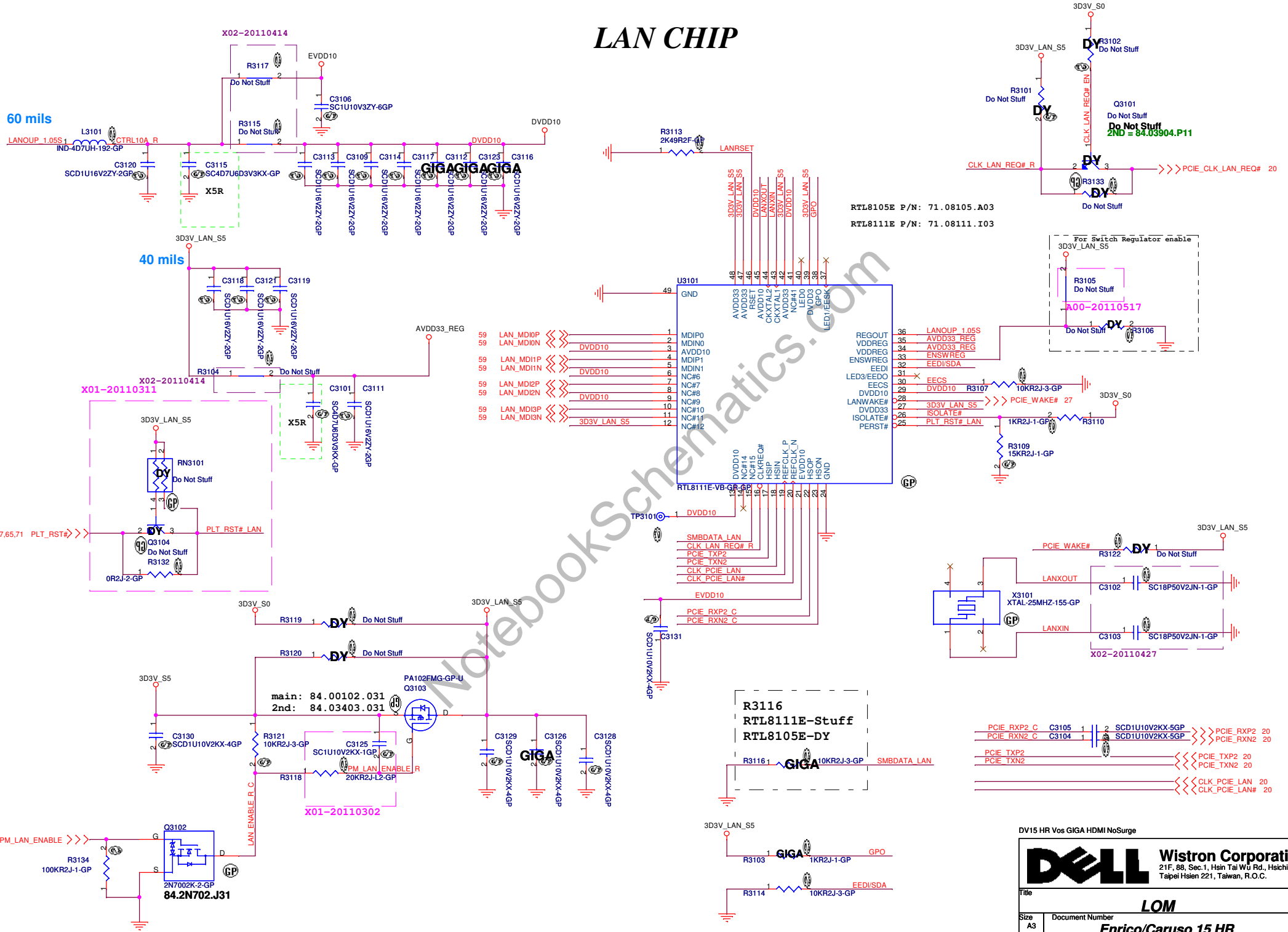


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LAN CHIP

60 mils

40 mils



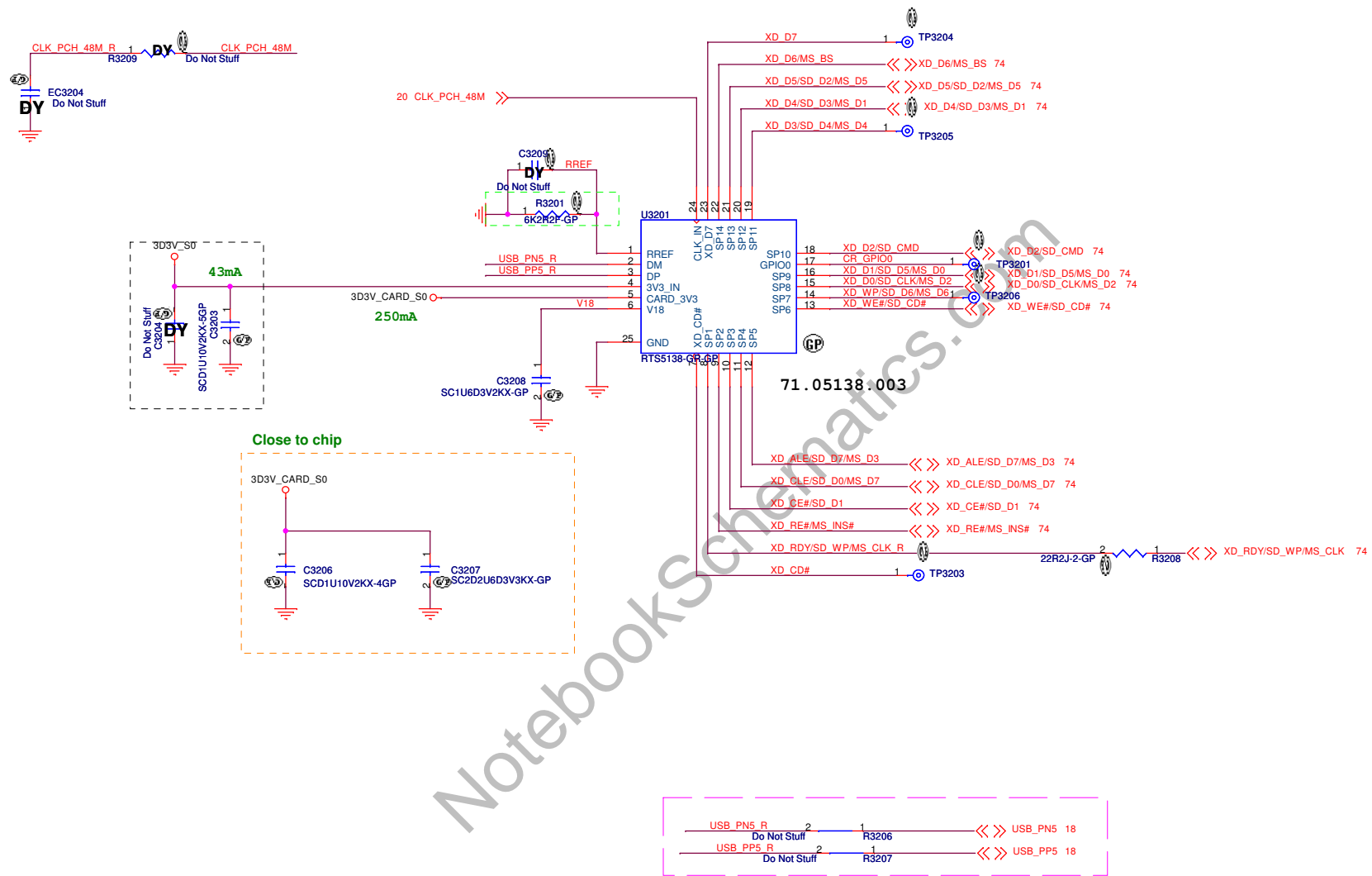
DV15 HR Vos GIGA HDMI NoSurge

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LOM**

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SSID = SDIO



A00-20110530

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Title Card Reader-RTS5138		
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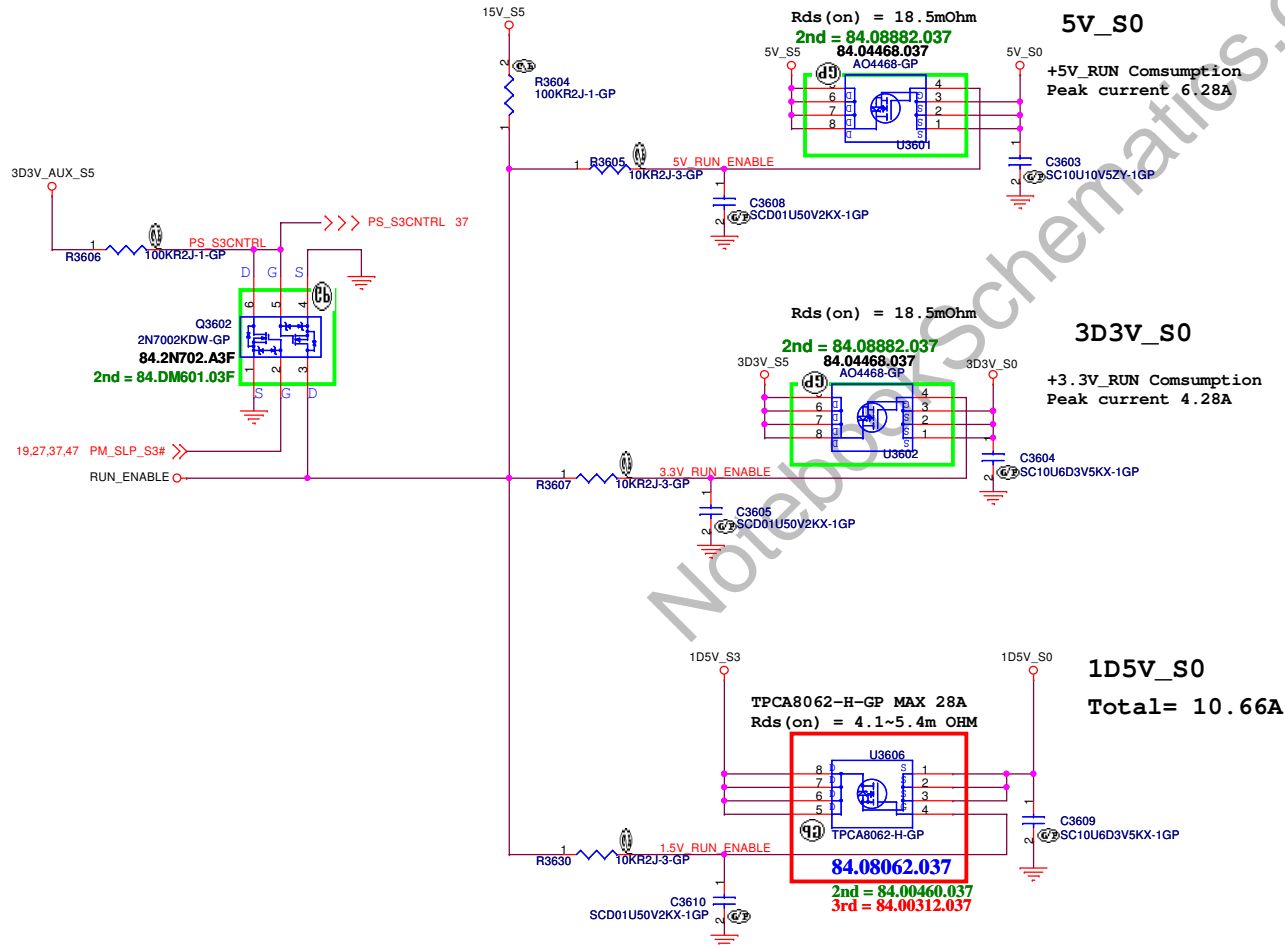
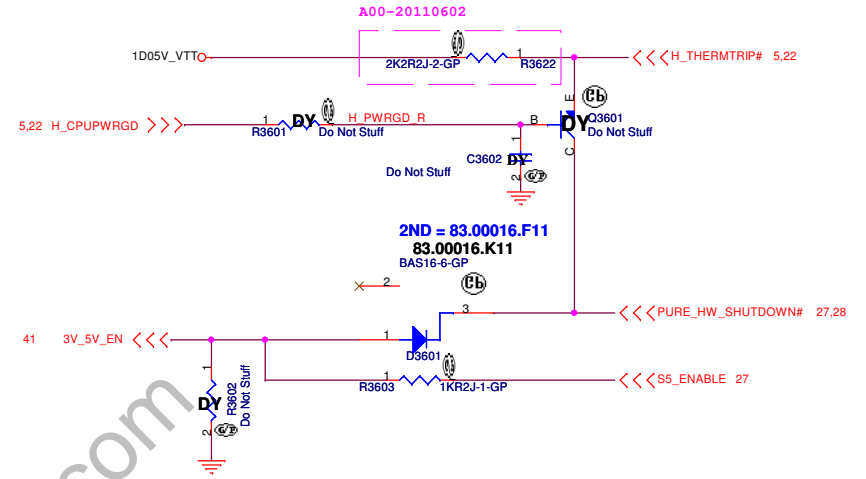
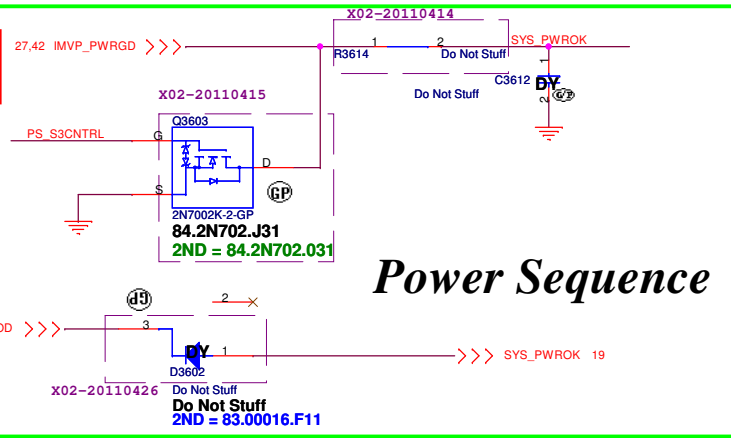
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DV15 HR Vos GIGA HDMI NoSurge



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Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
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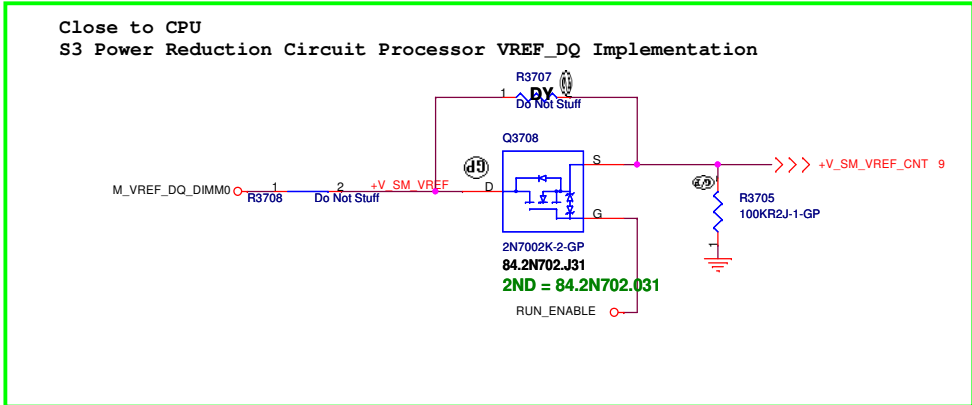
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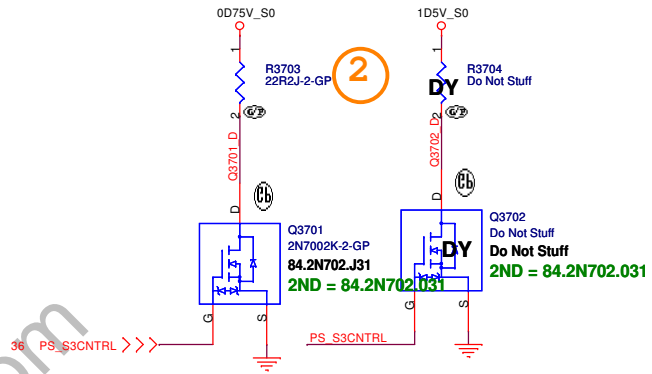
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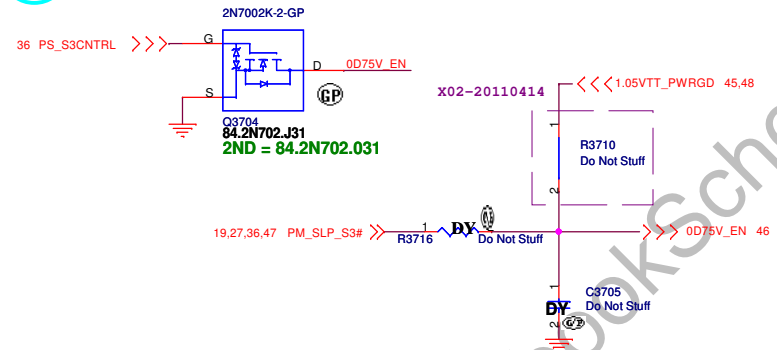
Title Power Plane Enable		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
Date: Thursday, June 02, 2011	Sheet 36 of 104	



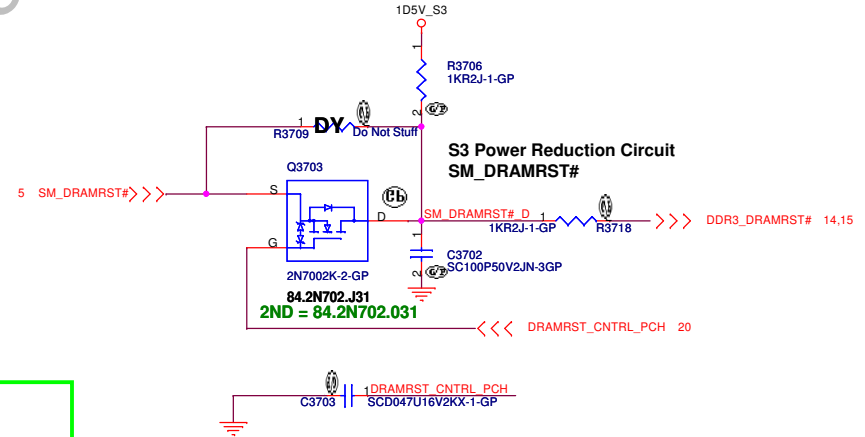
**Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK**



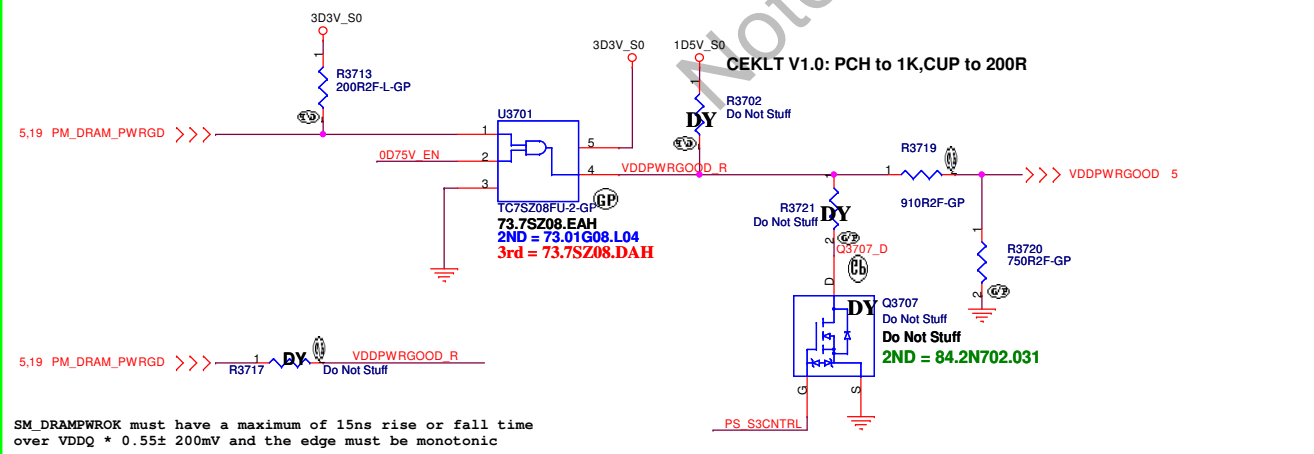
5 S3 Power Reduction



**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**



**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

DV15 HR Vos GIGA HDMI NoSurge

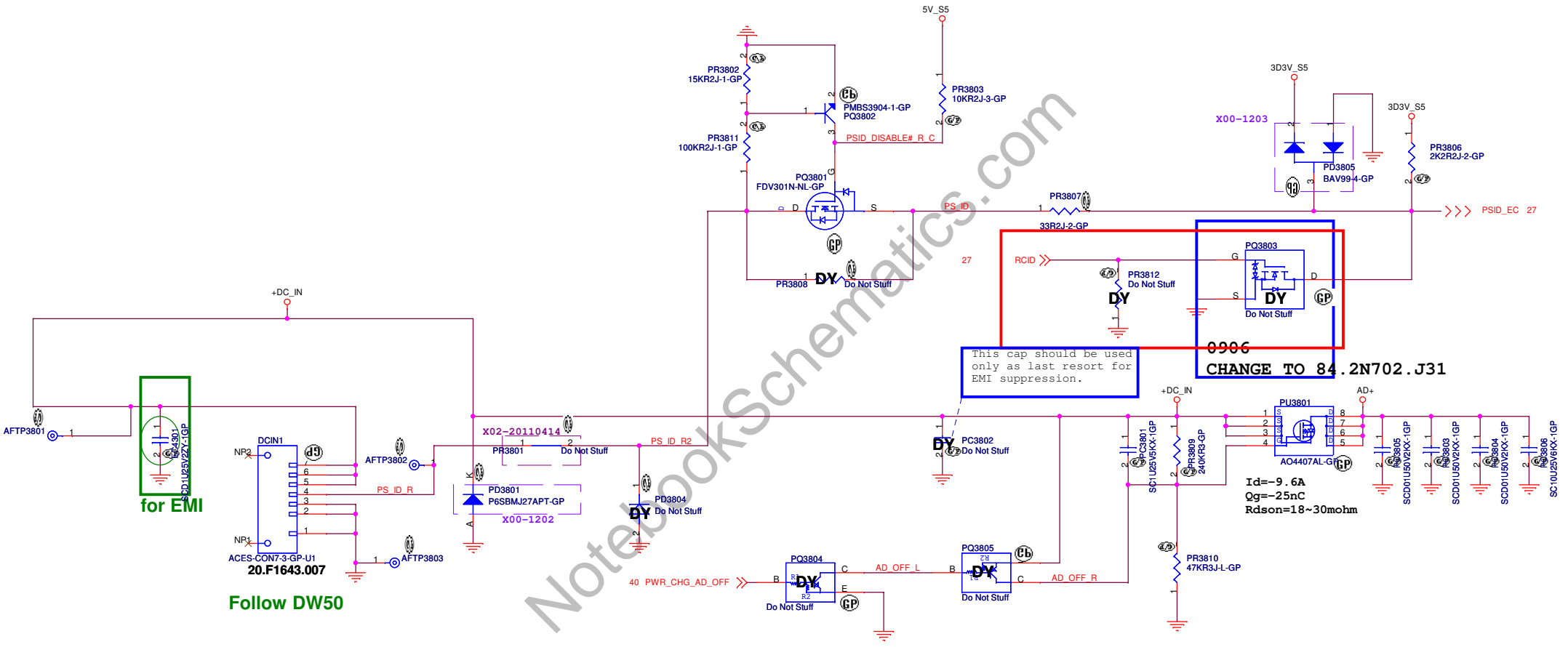
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER**

Size A3	Document Number	Rev
Date: Thursday, June 02, 2011	Enrico/Caruso 15 HR	X01
	Sheet 37 of	104

SSID = PWR.Support

DCin CONN



for EMI

Follow DW50

This cap should be used only as last resort for EMI suppression.

CHANGE TO 84.2N702.J31

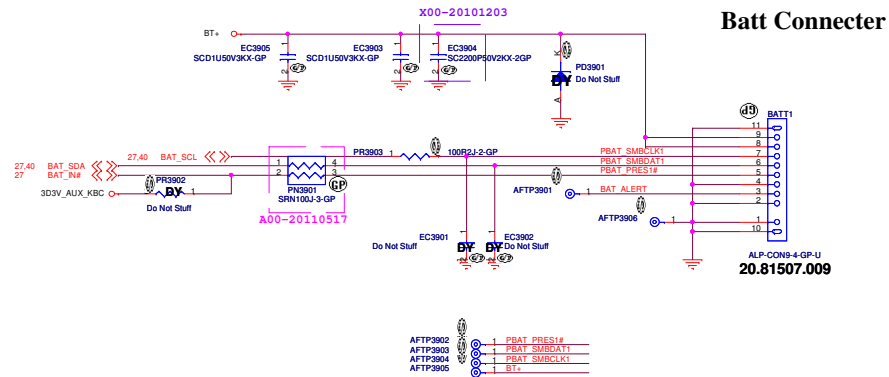
Id=-9.6A
 Qg=-25nC
 Rds(on)=18~30mohm

DV15 HR Vos GIGA HDMI NoSurge

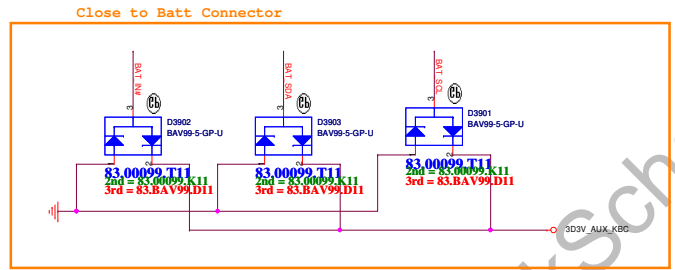
Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN**

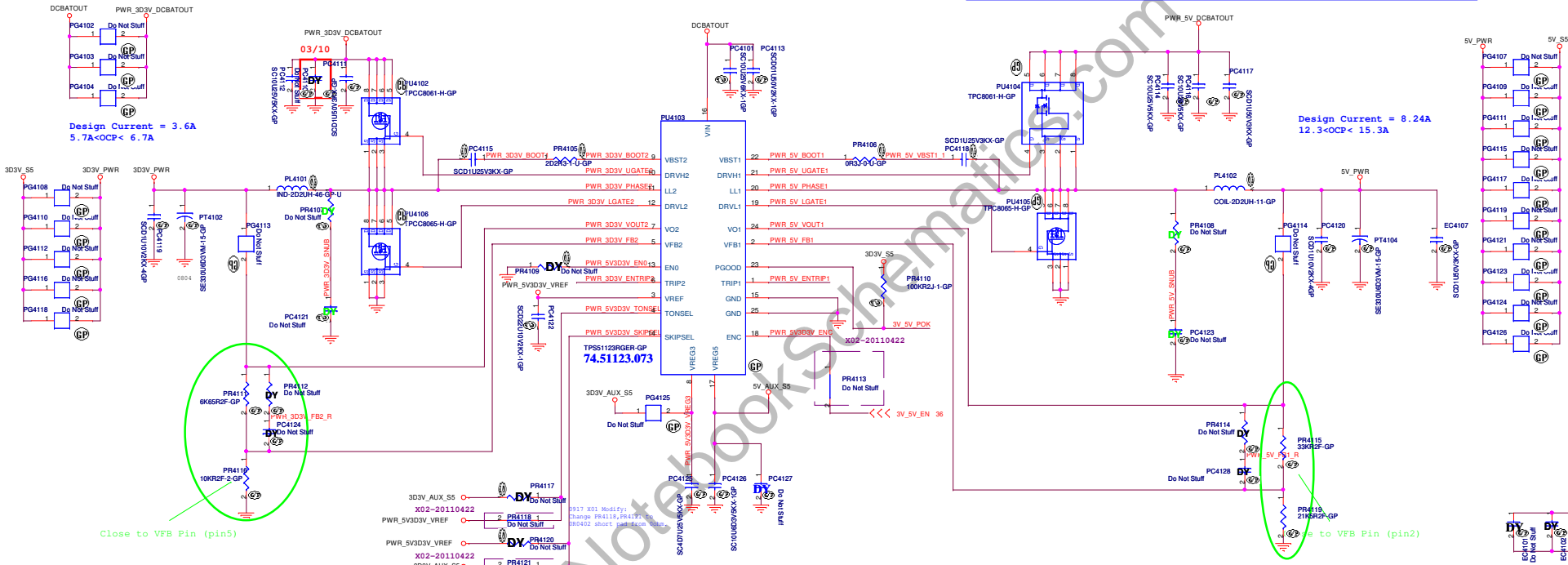
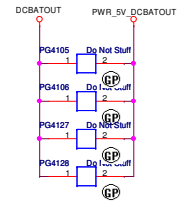
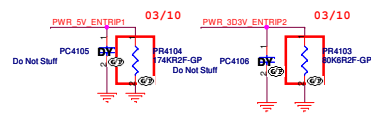
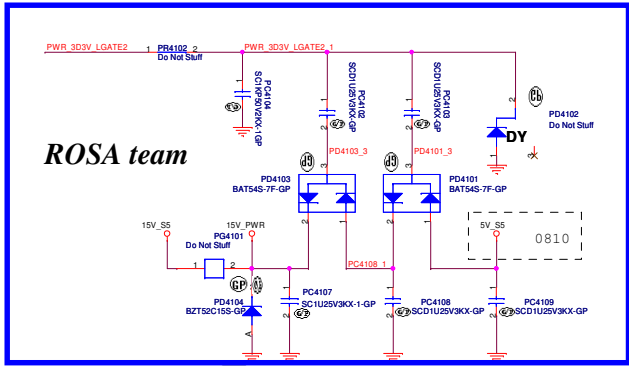
Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
Date: Thursday, June 02, 2011	Sheet 38 of 104	



For actual location, need to be swap all pin



SSID = PWR.Plane.Regulator_5v3p3v

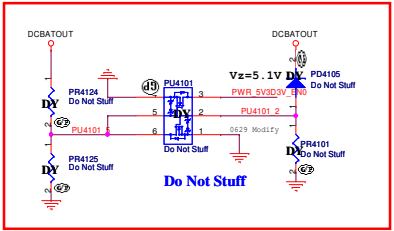


Design Current = 3.6A
5.7A < OCP < 6.7A

Design Current = 8.24A
12.3 < OCP < 15.3A

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 2.20UH PCMC104T-2R2 Cynotec 7mohm Isat =27Arms 68.2R210.20C
 O/P cap: 330U6.3V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
 H/S: TPCC8061-H / 21mohm/30mohm@4.5Vgs/ 84.08061.037
 L/S: TPCC8065-H / 12mohm/15mohm@4.5Vgs/ 84.08065.037

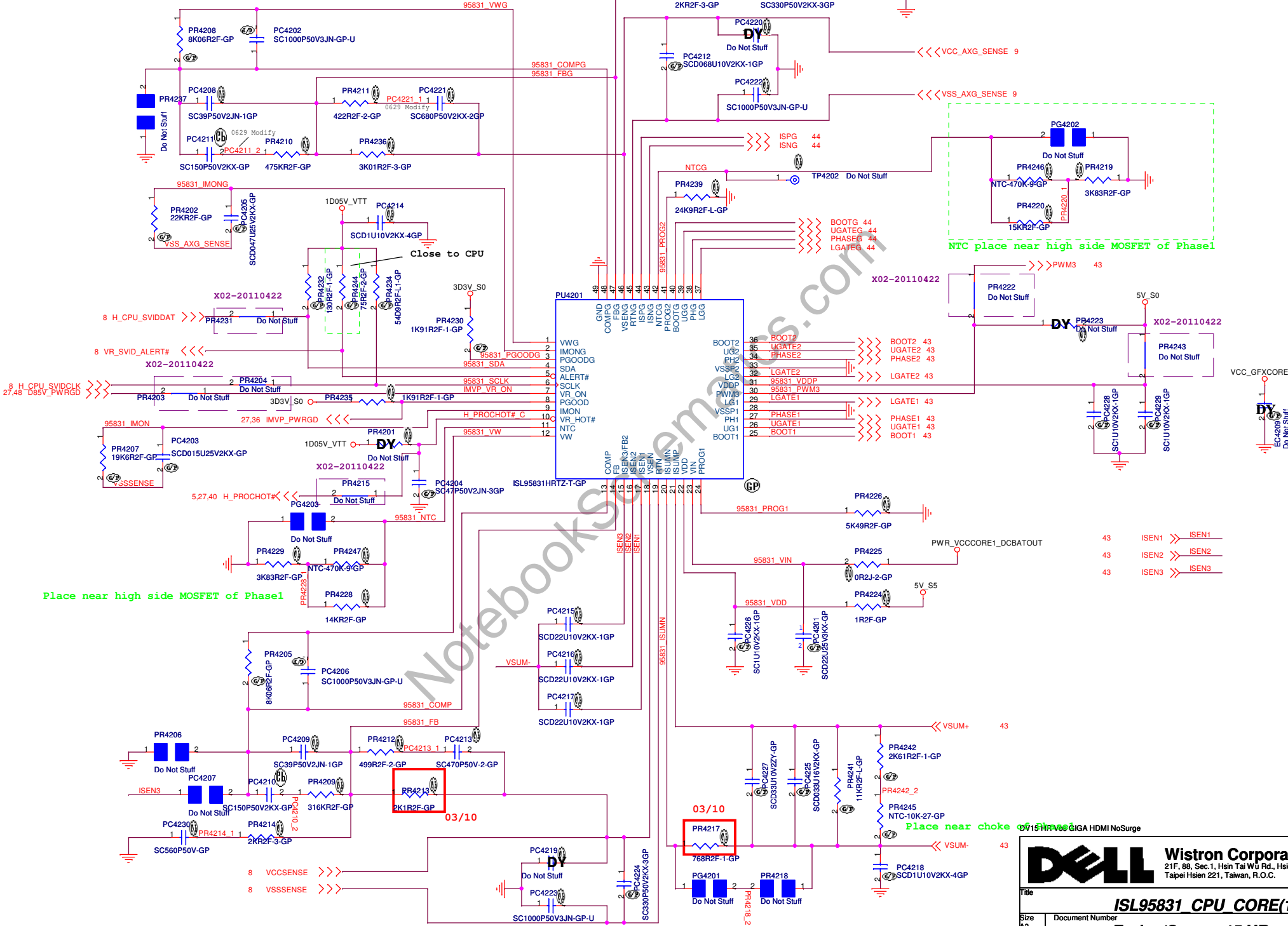
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 2.2U PCMC063T-2R2MN Cynotec 20mohm Isat =14Arms 68.2R210.20B
 O/P cap: 330U6.3V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
 H/S: TPCC8061-H NC 8P / 21mohm/29mohm@4.5Vgs/ 84.08061.A37
 L/S: TPCC8065-H NC 8P / 12.1mohm/17.4mohm@4.5Vgs/ 84.08065.A37

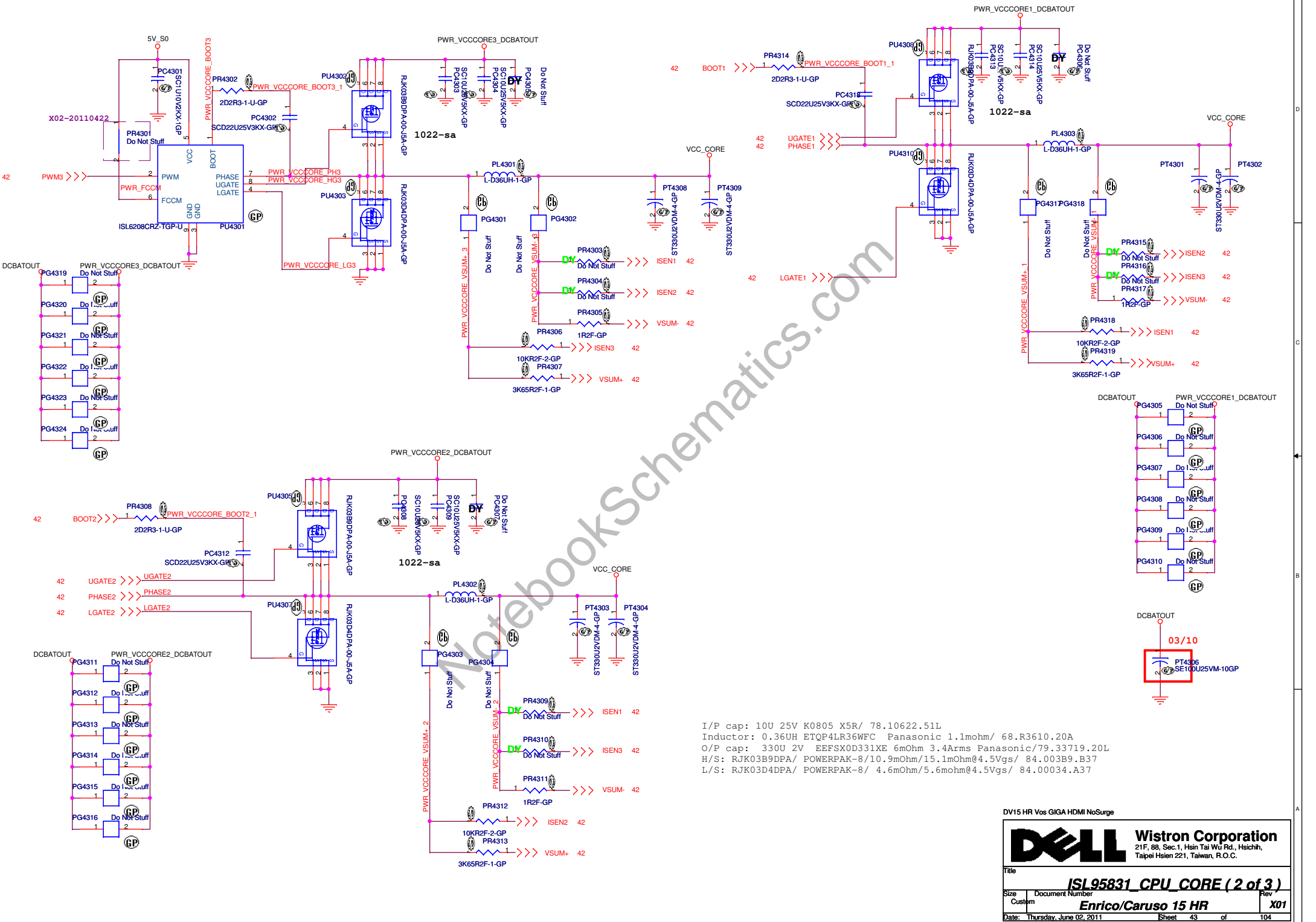
DV15 HR Vos GIGM HDNoSurge

Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.

File: 5V/3D3V(TPS51123RGER)
 Size: Document Number
 A2: Enrico/Caruso 15 HR X01
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SSID = CPU.Regulator





I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A
 O/P cap: 330U 2V EEP5X0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

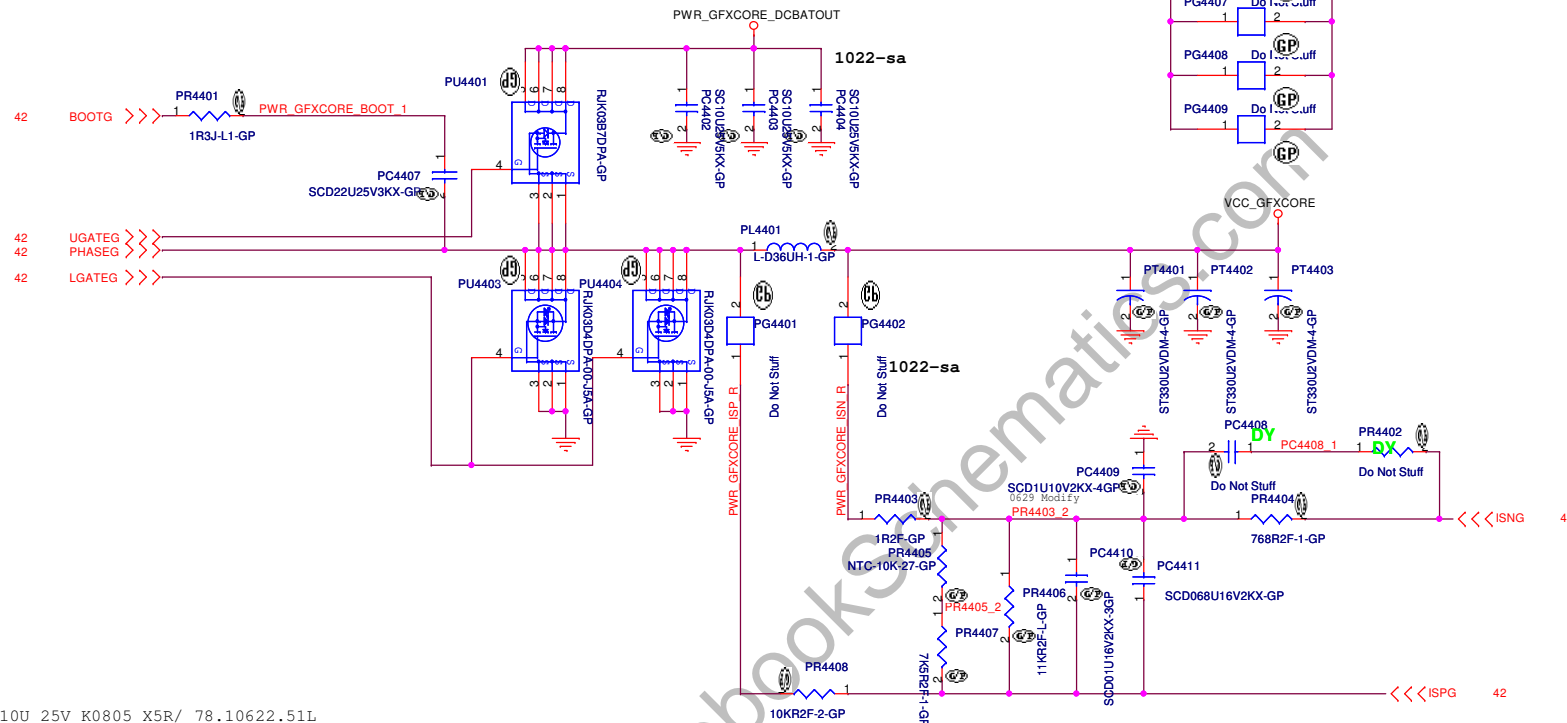
DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL95831 CPU CORE (2 of 3)**

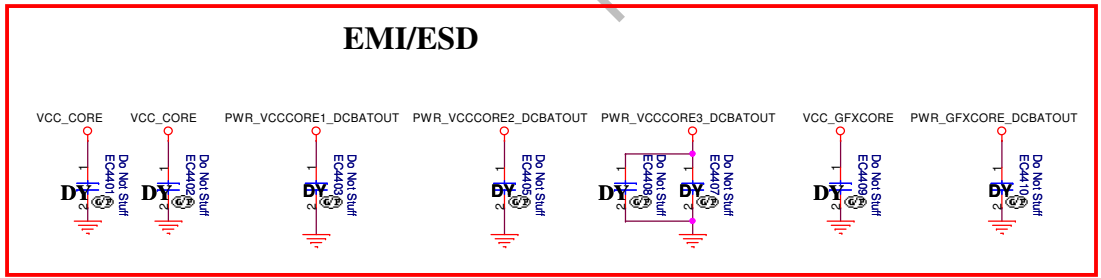
Size	Document Number	Rev
Custom	Enrico/Caruso 15 HR	X01

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VCC_GFXCORE
 I_{omax}=33A
 OCP>50A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 0.36UH ETQP4LR36WFC Panasonic 1.1mohm/ 68.R3610.20A
 O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
 H/S: RJK03B7DPA NC WPAK 8P/7.7mOhm/10.7mOhm@4.5Vgs/84.003B7.037
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37



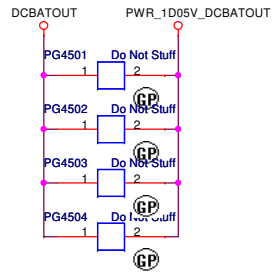
DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

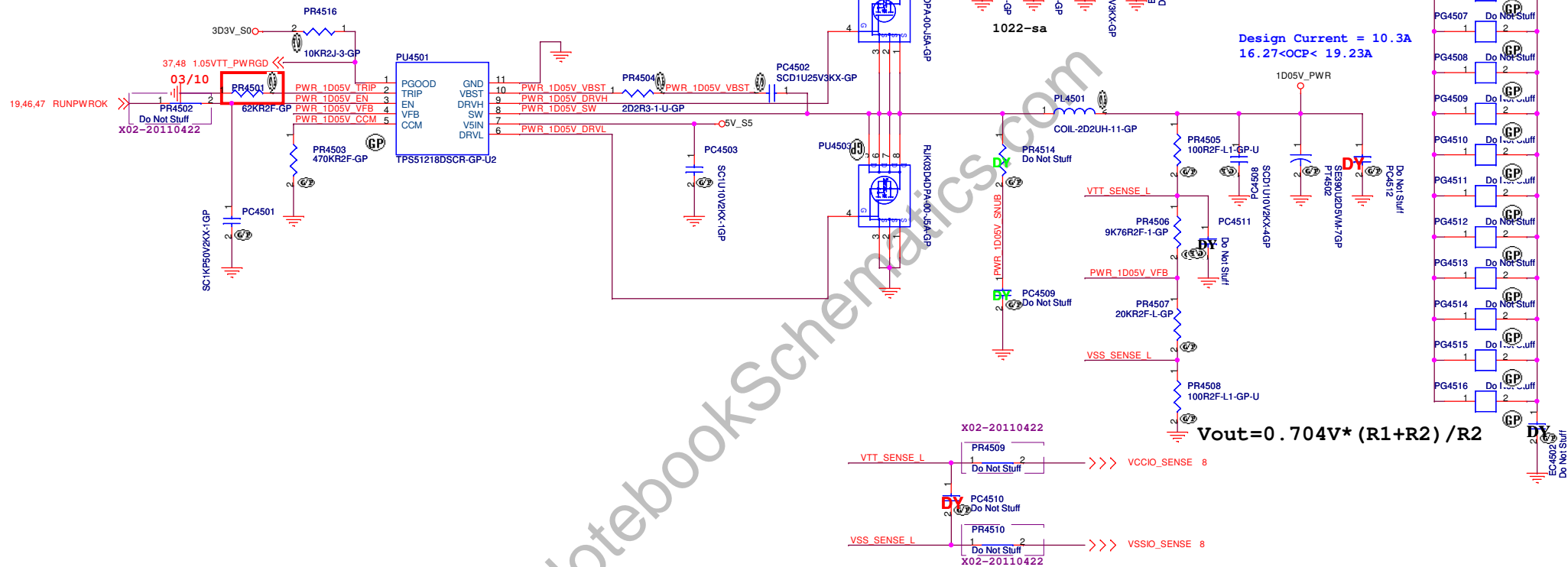
Title: **ISL95831 CPU CORE(3/3)**

Size A3	Document Number	Rev
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TPS51218 for 1D05V



Design Current = 10.3A
16.27 < OCP < 19.23A

$$V_{out} = 0.704V * (R1 + R2) / R2$$

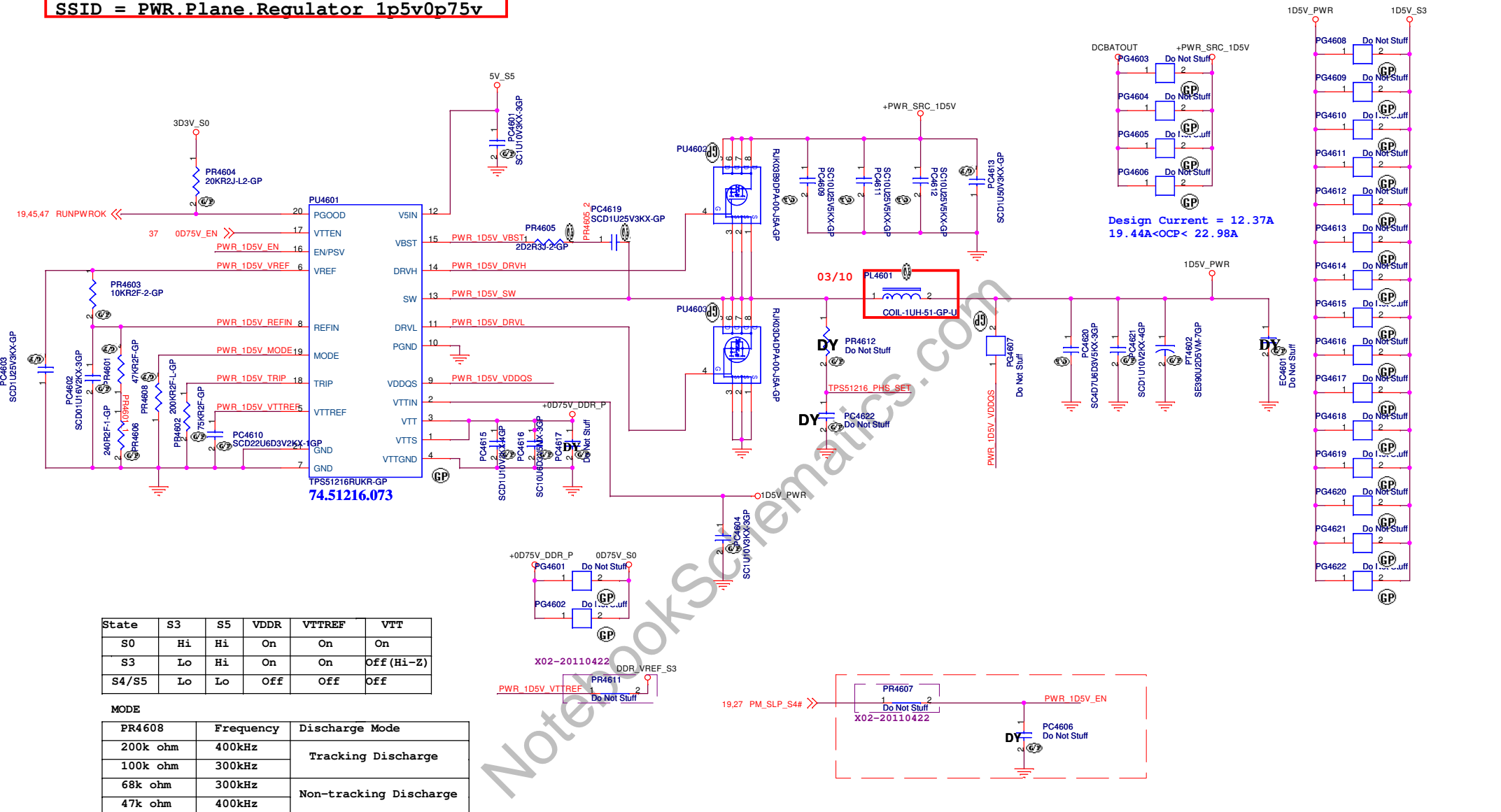
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 2.20UH PCMC104T-2R2 Cynotec 7mohm Isat =27Arms 68.2R210.20C
 O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge



Title TPS51218 +1.05V VTT		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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SSID = PWR.Plane.Regulator 1p5v0p75v



Design Current = 12.37A
19.44A < OCP < 22.98A

74.51216.073

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR4608	400kHz	Tracking Discharge
200k ohm	300kHz	
100k ohm	300kHz	Non-tracking Discharge
68k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: 1.0UH PCB104T-1R0M Cyntec 3mohm Isat =28Arms 68.1R01C.10Q
 O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
 H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
 L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

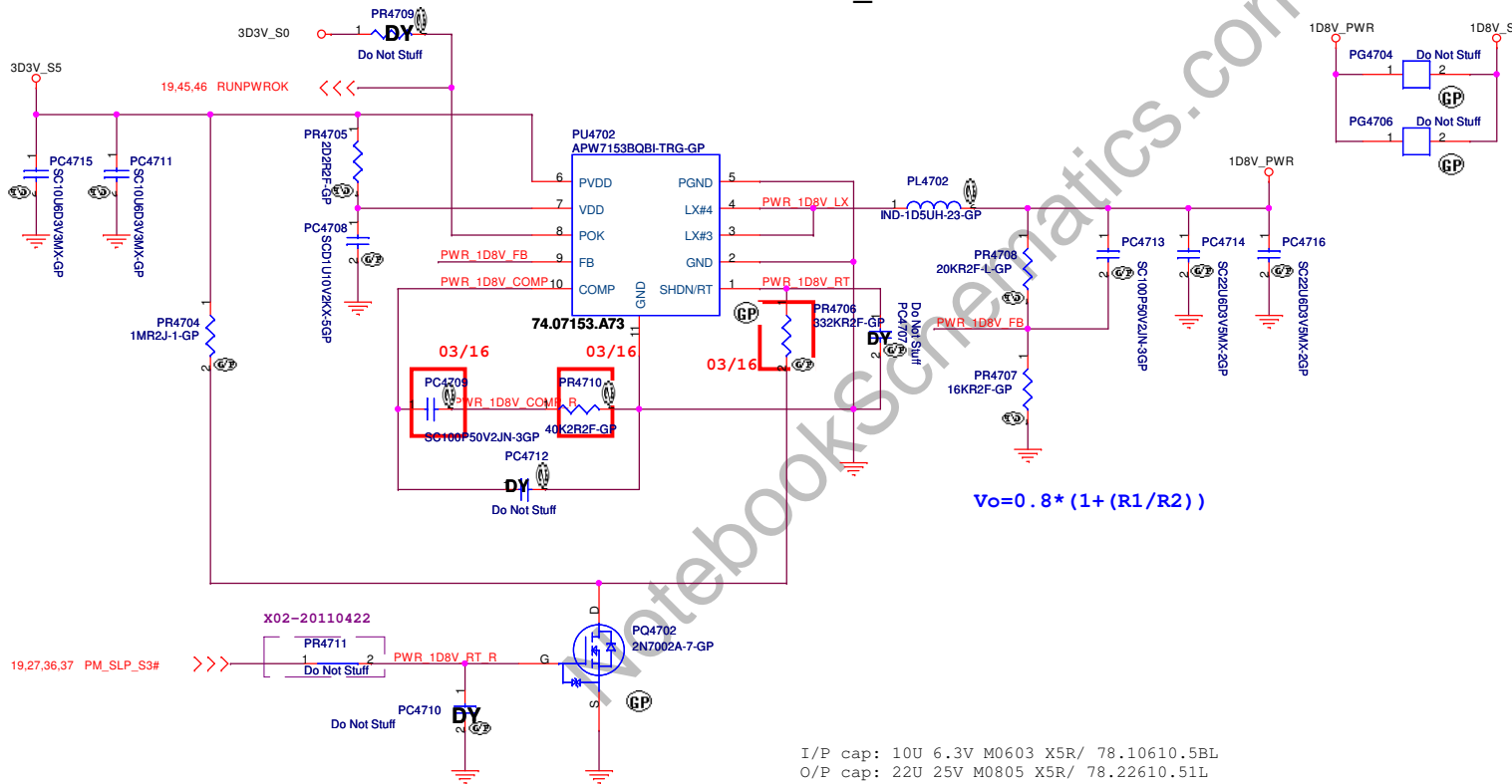
DV15 HR Vos GIGA HDMI NoSurge



SSID = PWR.Plane.Regulator_1D8V_S0

APW7153B for 1D8V_S0

+1.8V_RUN
Design current = 0.87A

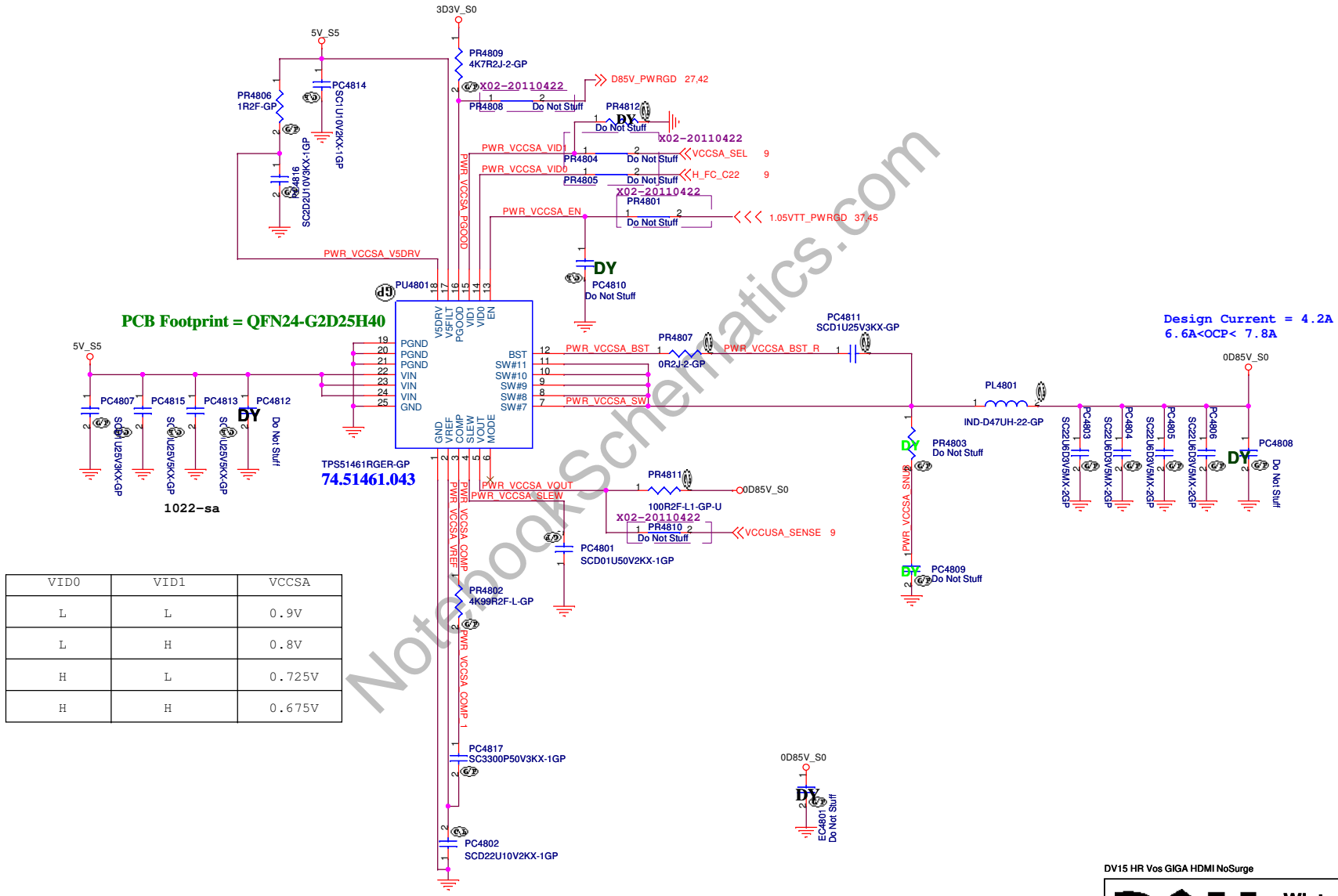


I/P cap: 10U 6.3V M0603 X5R/ 78.10610.5BL
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: 1.5U PCMC063T Cynotec 14mohm/15mohm Isat =18Arms 68.1R510.10K

DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title TPS51311 for 1D8V_S0	
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TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

Design Current = 4.2A
6.6A < OCP < 7.8A

DV15 HR Vos GIGA HDMI NoSurge

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

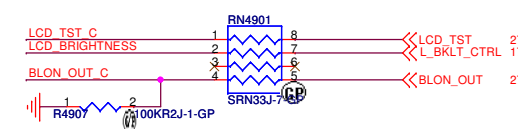
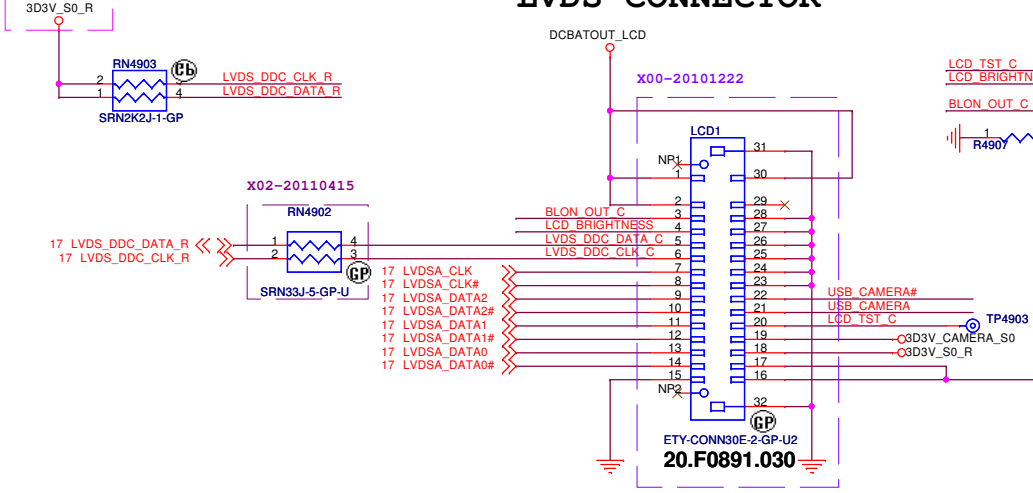
Title: **TPS51461 VCCSA**

Size A3	Document Number	Rev
Date: Thursday, June 02, 2011	Enrico/Caruso 15 HR	X01

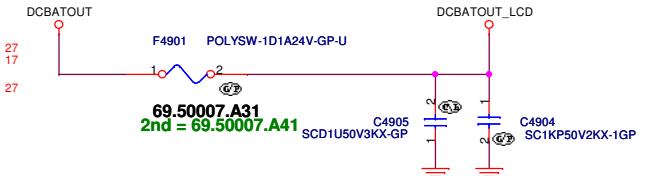
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X01-20110307

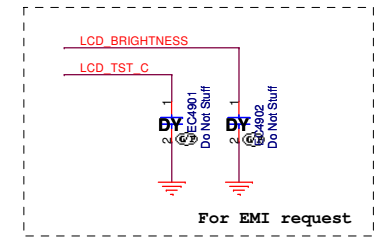
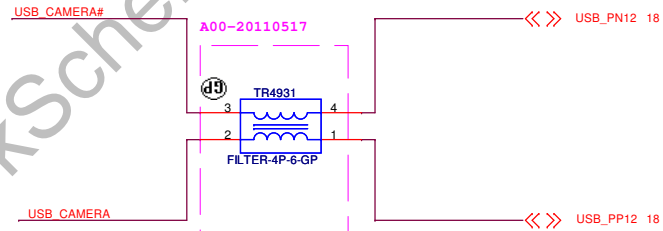
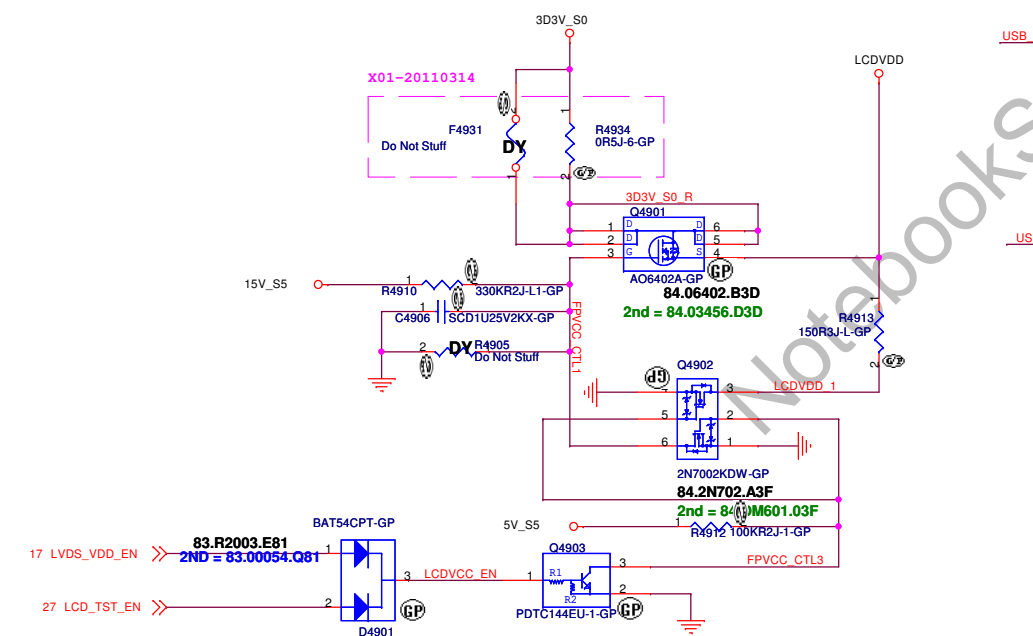
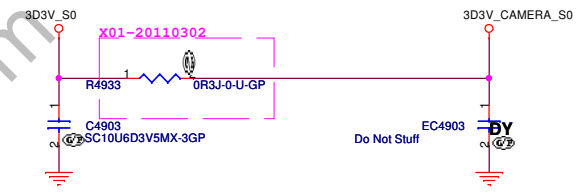
LVDS CONNECTOR



INVERTER POWER



Camera Power



DV15 HR Vos GIGA HDMI NoSurge

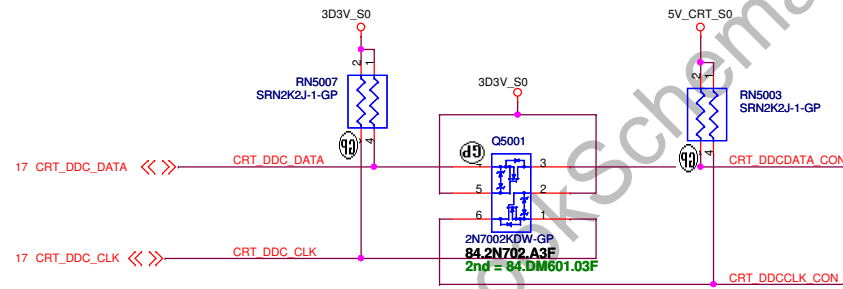
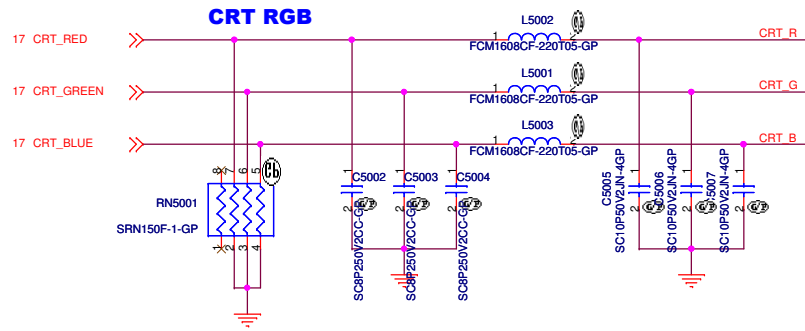


File			LCD Connector		
Size	Document Number		Rev		
A3	Enrico/Caruso 15 HR		X01		
Date:	Thursday, June 02, 2011	Sheet	49	of	104

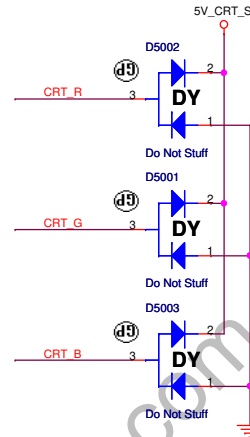
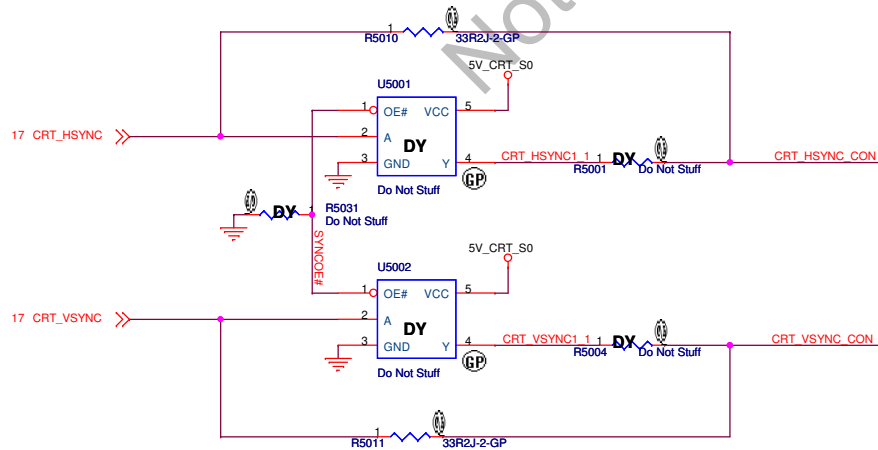
SSID = VIDEO

Layout Note:

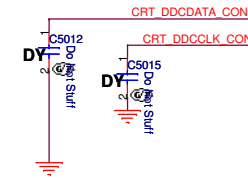
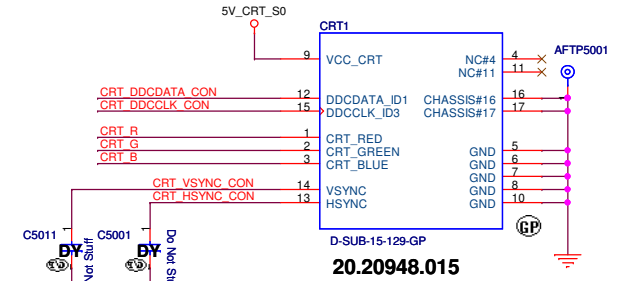
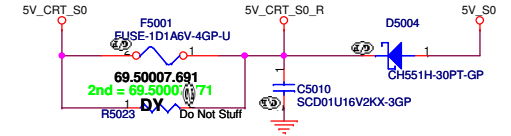
- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync



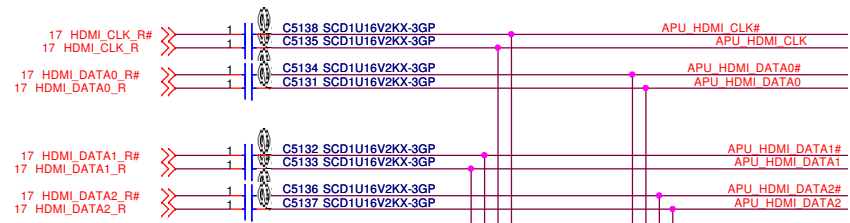
- AFTP5002 1 5V_CRT_S0
- AFTP5003 1 CRT_DDCDATA_CON
- AFTP5004 1 CRT_DDCCLK_CON
- AFTP5005 1 CRT_R
- AFTP5006 1 CRT_G
- AFTP5007 1 CRT_B
- AFTP5008 1 CRT_HSYNC_CON
- AFTP5009 1 CRT_VSYNC_CON



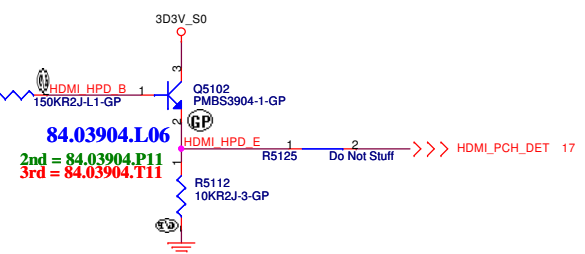
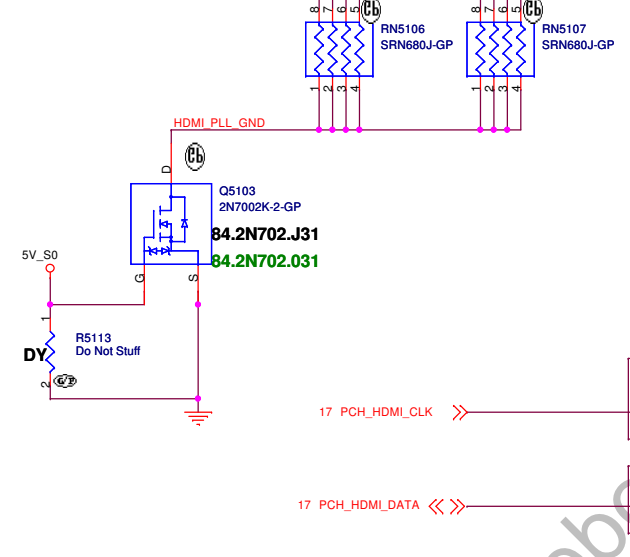
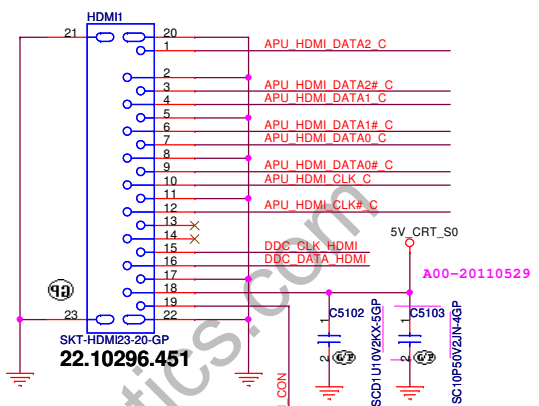
DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		CRT Connector	
Title	Document Number	Rev	
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SSID = VIDEO



HDMI CONN



APU HDMI_DATA1	1	2	APU HDMI_DATA1_C	APU HDMI_CLK	1	2	APU HDMI_CLK_C
Do Not Stuff			R5146	Do Not Stuff			R5144
APU HDMI_DATA1#	1	2	APU HDMI_DATA1#_C	APU HDMI_CLK#	1	2	APU HDMI_CLK#_C
Do Not Stuff			R5147	Do Not Stuff			R5145
APU HDMI_DATA2	1	2	APU HDMI_DATA2_C	APU HDMI_DATA0	1	2	APU HDMI_DATA0_C
Do Not Stuff			R5148	Do Not Stuff			R5143
APU HDMI_DATA2#	1	2	APU HDMI_DATA2#_C	APU HDMI_DATA0#	1	2	APU HDMI_DATA0#_C
Do Not Stuff			R5142	Do Not Stuff			R5141

A00-20110530

DV15 HR Vos GIGA HDMI NoSurge



Title HDMI Level Shifter/Connector		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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NotebookSchematics.com

DV15 HR Vos GIGA HDMI NoSurge



Title		
Reserved		
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(Blanking)

NotebookSchematics.com

DV15 HR Vos GIGA HDMI NoSurge



Title		
LVDS Switch		
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NotebookSchematics.com

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Reserved		
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A3	Enrico/Caruso 15 HR	X01
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SSID = User.Interface

(Blanking)

NotebookSchematics.com

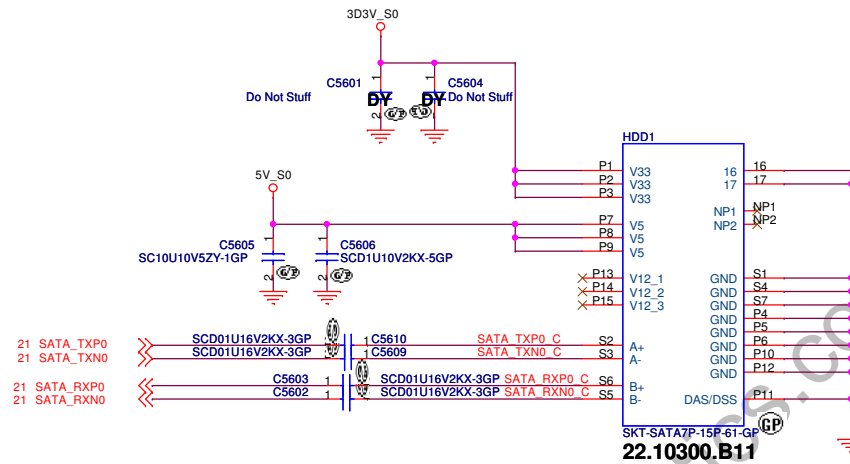
DV15 HR Vos GIGA HDMI NoSurge



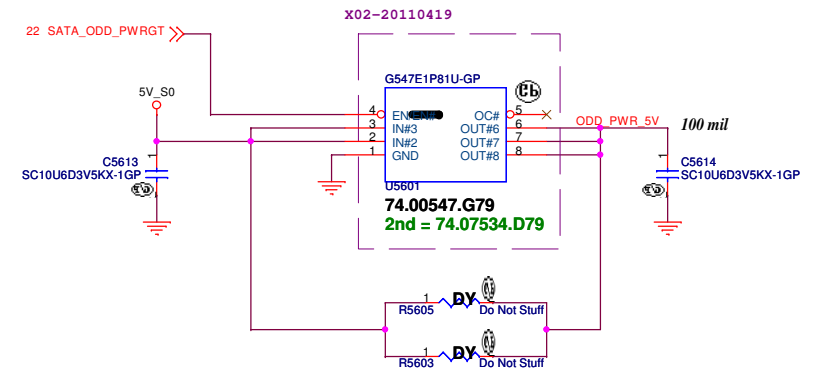
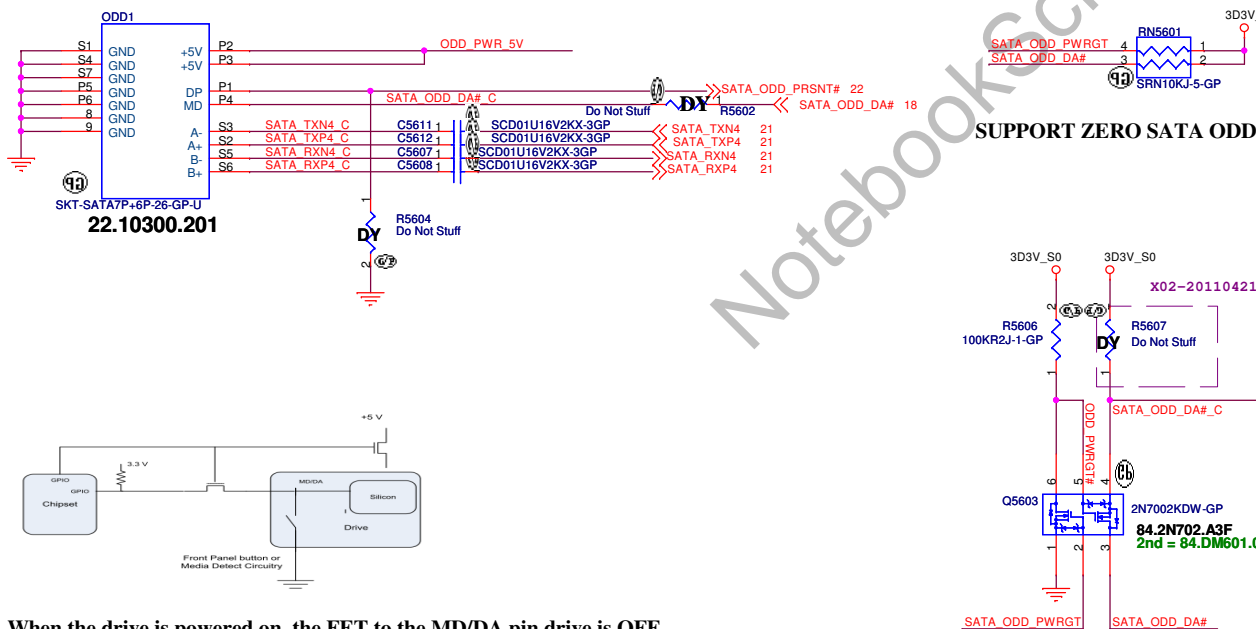
Title		
ITP/Fan Connector		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
Date: Thursday, June 02, 2011	Sheet 55 of	104

SSID = SATA

SATA HDD Connector



ODD Connector



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

DV15 HR Vos GIGA HDMI NoSurge



Title HDD/ODD			
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01	
Date: Thursday, June 02, 2011	Sheet 56	of	104

SSID = ESATA

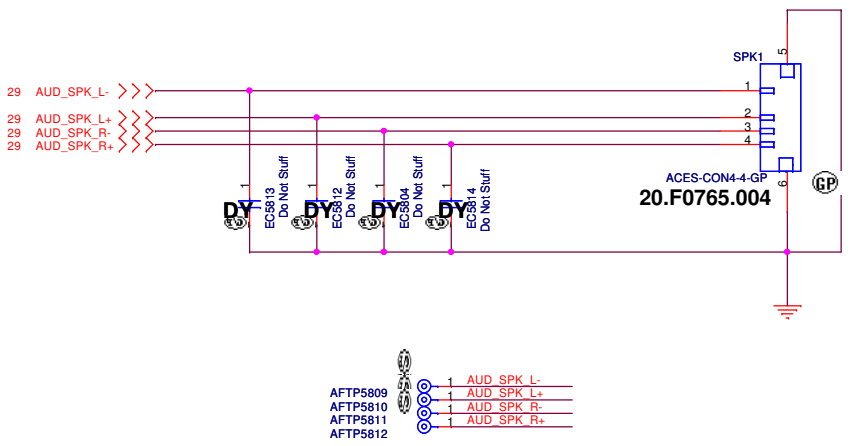
NotebookSchematics.com

DV15 HR Vos GIGA HDMI NoSurge

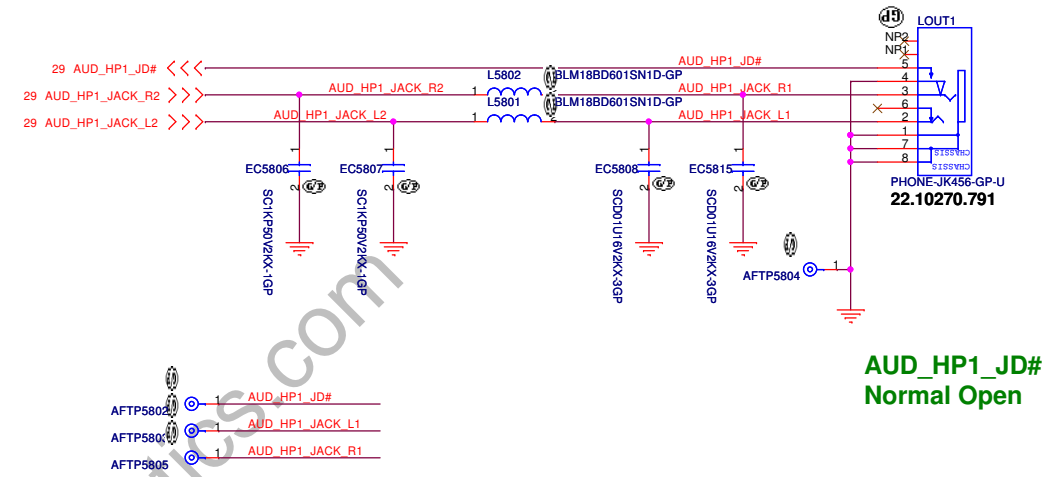
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		ESATA	
Size A3	Document Number	Enrico/Caruso 15 HR	Rev X01
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SSID = AUDIO

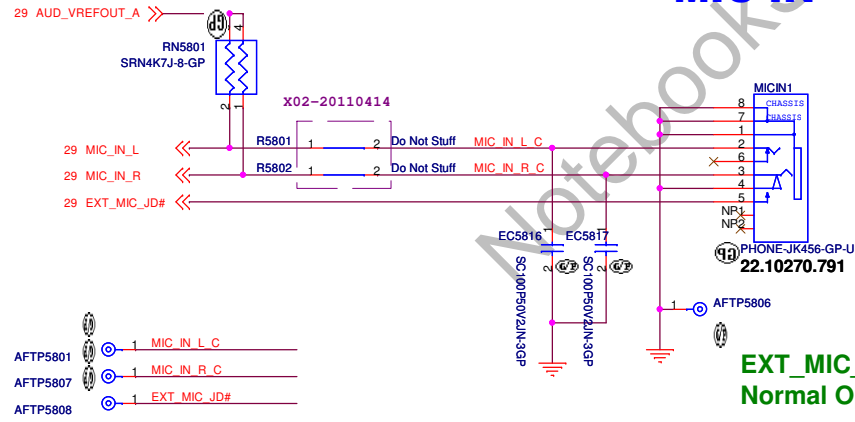
Speaker Connector



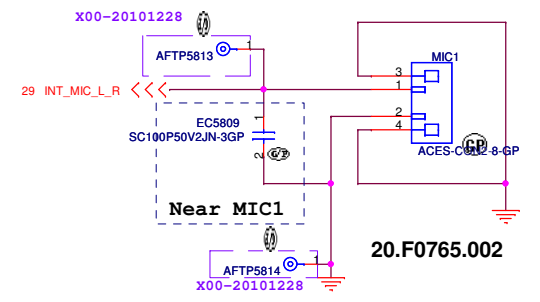
LINE1 OUT



MIC IN



Internal Microphone



DV15 HR Vos GIGA HDMI NoSurge

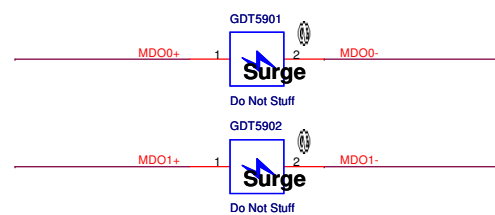
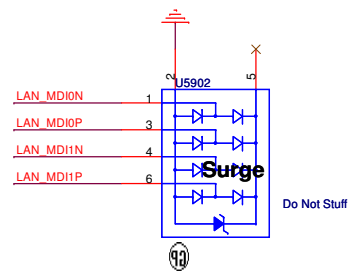
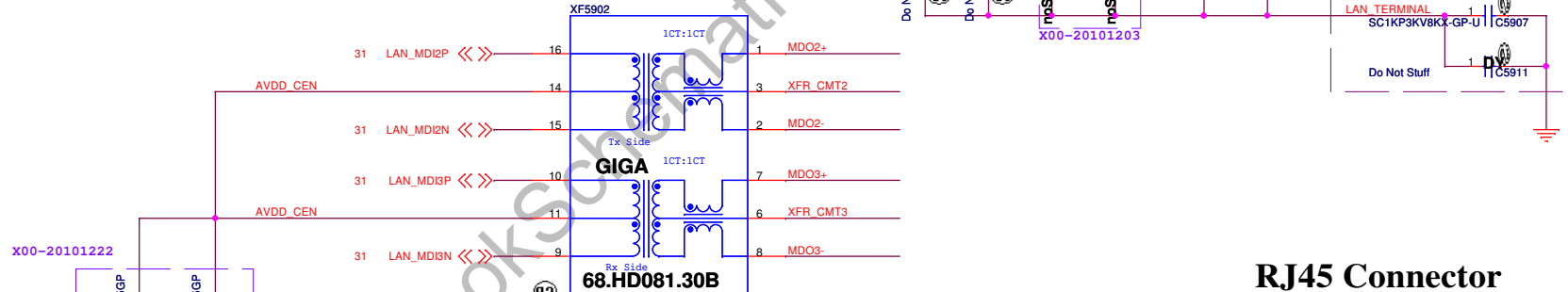
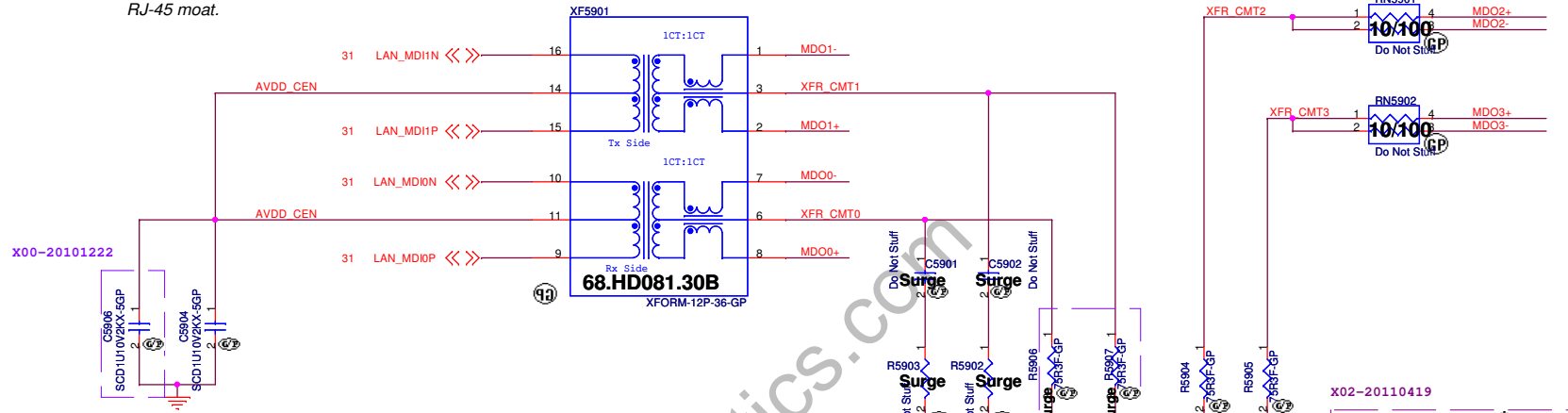
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **SPEAKER CONN**

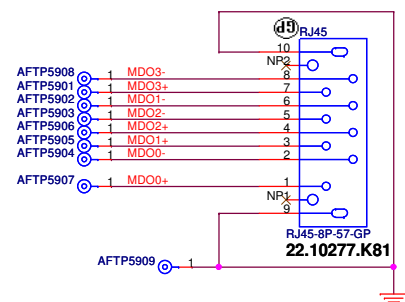
Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
Date: Thursday, June 02, 2011	Sheet: 58	of: 104

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

10/100M Lan Transformer



RJ45 Connector



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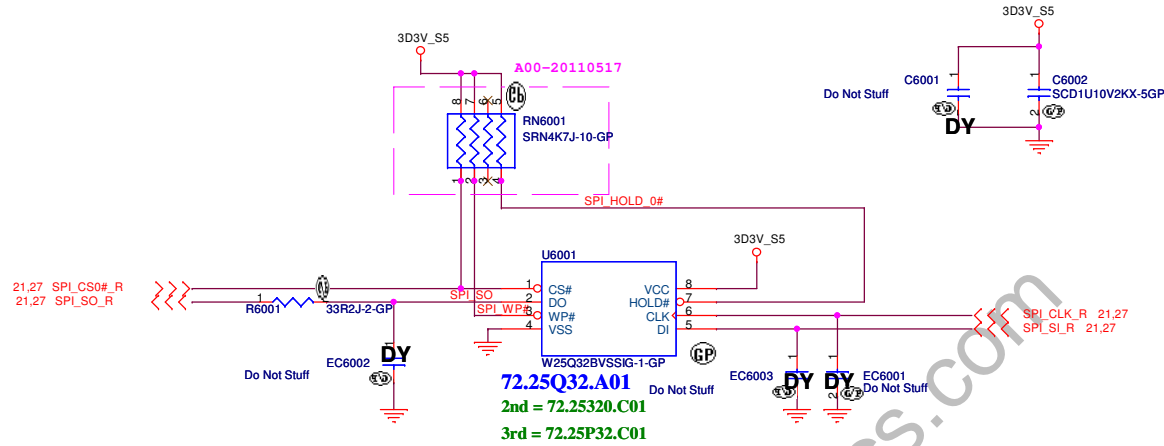
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

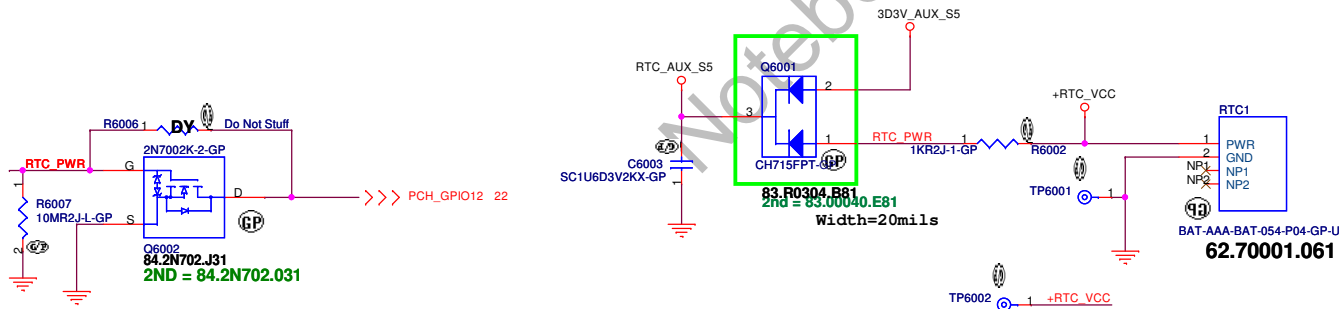
Size: A3	Document Number: Enrico/Caruso 15 HR	Rev: X01
Date: Thursday, June 02, 2011	Sheet: 59 of 104	

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



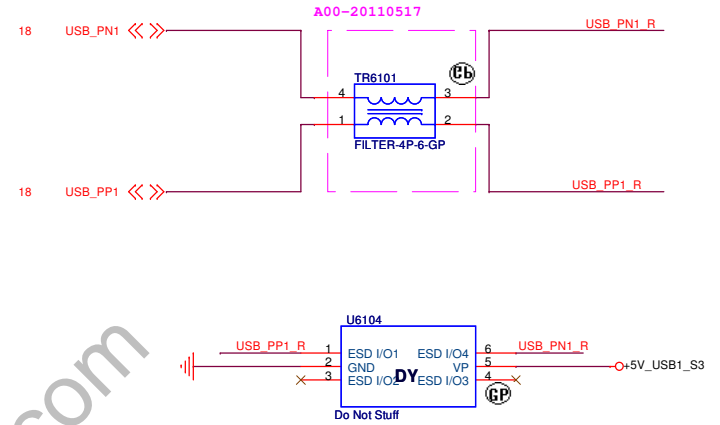
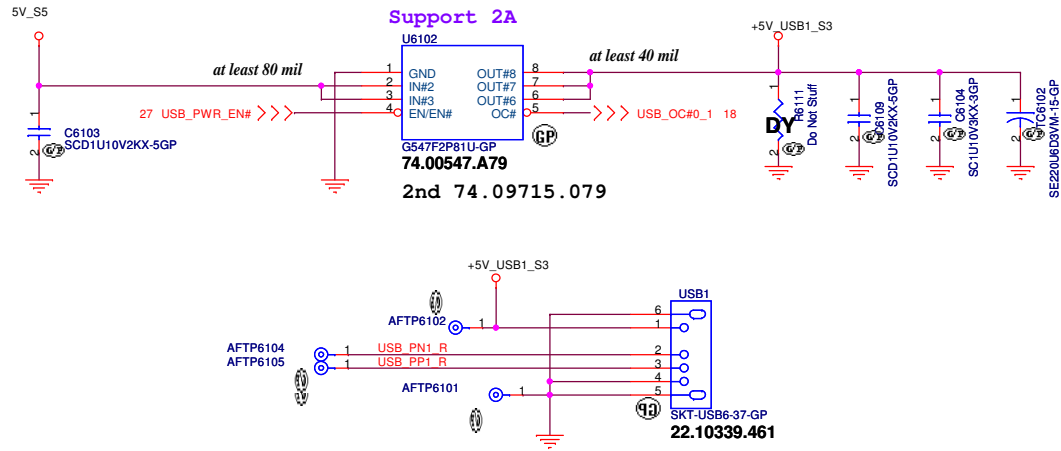
DV15 HR Vos GIGA HDMI NoSurge

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

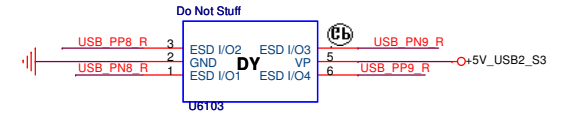
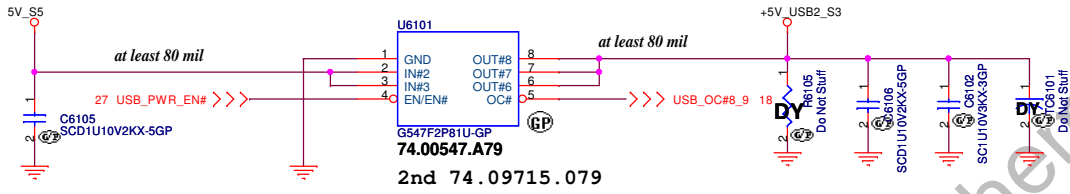
Title		
Flash/RTC		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
Date:	Thursday, June 02, 2011	Sheet 60 of 104

SSID = USB

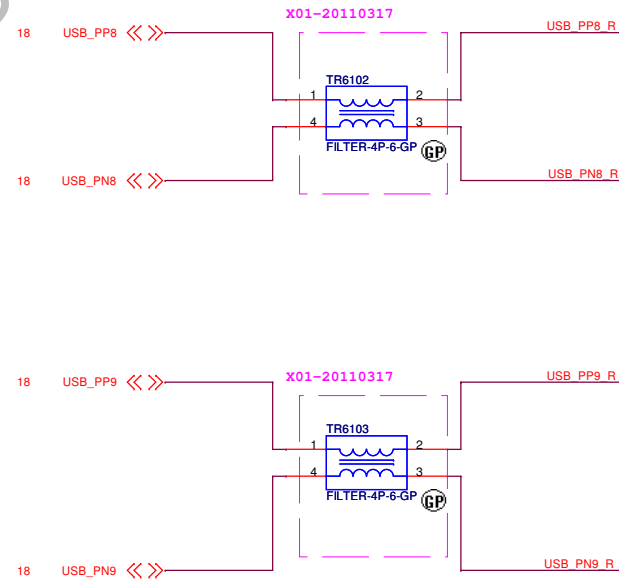
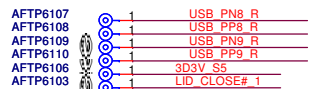
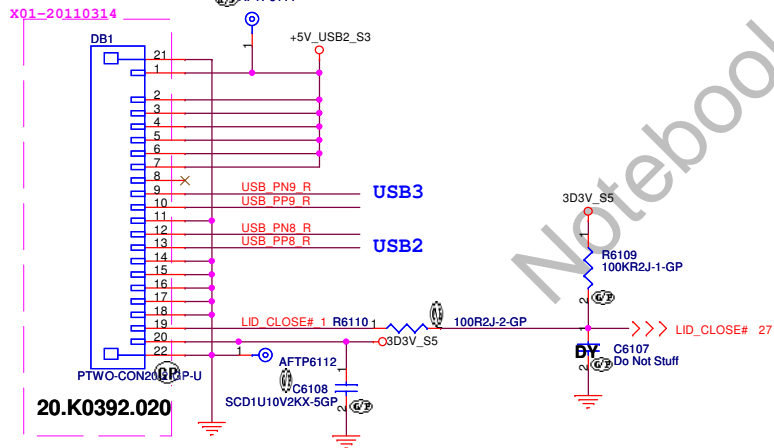
Left USB Power x1



Right USB Power x2



Pitch=0.5mm



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DV15 HR Vos GIGA HDMI NoSurge



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Reserved		
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SSID = User.Interface

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Title		
Bluetooth		
Size	Document Number	Rev
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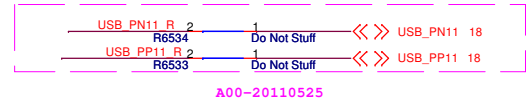
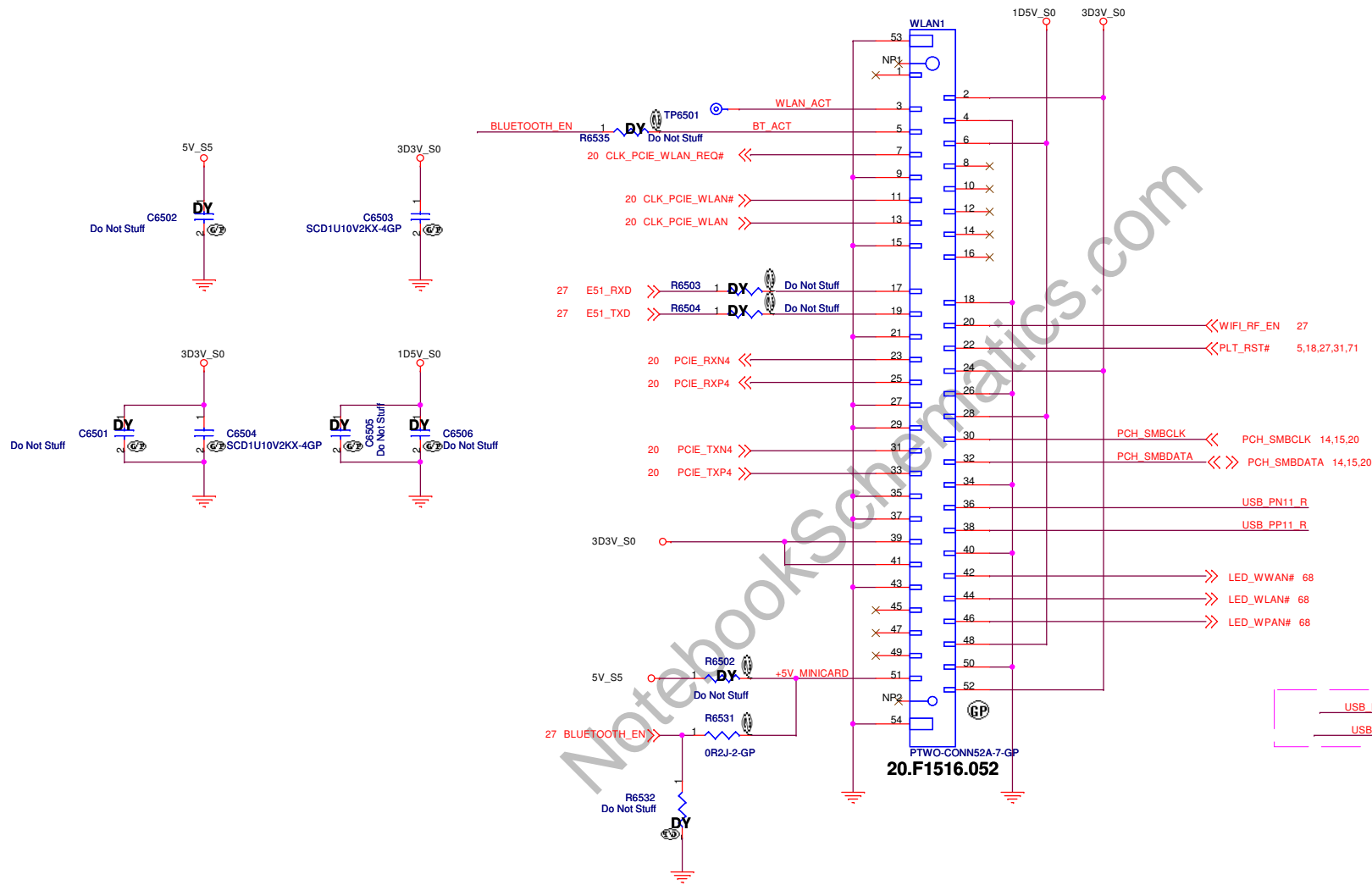


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Title		
RESERVED		
Size	Document Number	Rev
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SSID = Wireless

Mini Card Connector(802.11b/g/n)



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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title: RESERVED	
Size: A3	Document Number:	Rev: X01	
Date: Thursday, June 02, 2011	Sheet: 65 of 104		

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Reserved		
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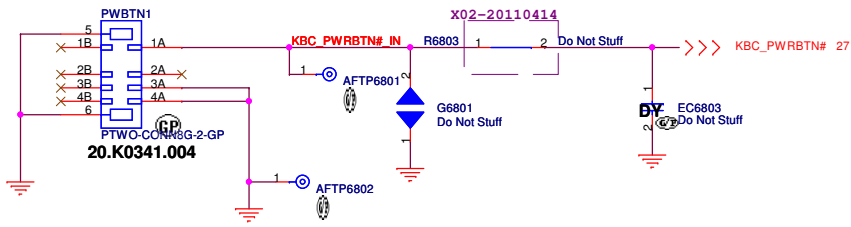
DV15 HR Vos GIGA HDMI NoSurge



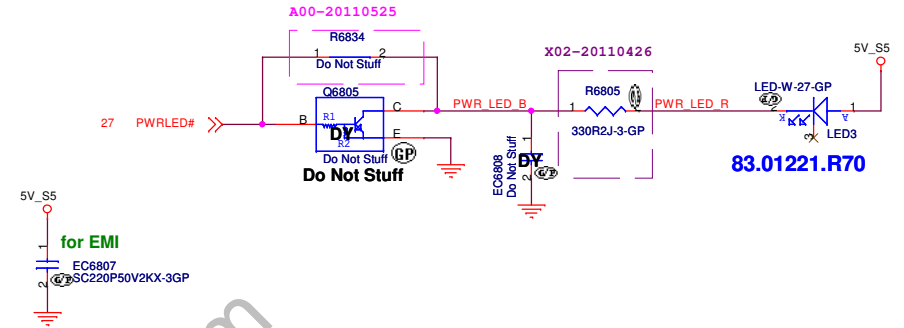
Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
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SSID = User.Interface

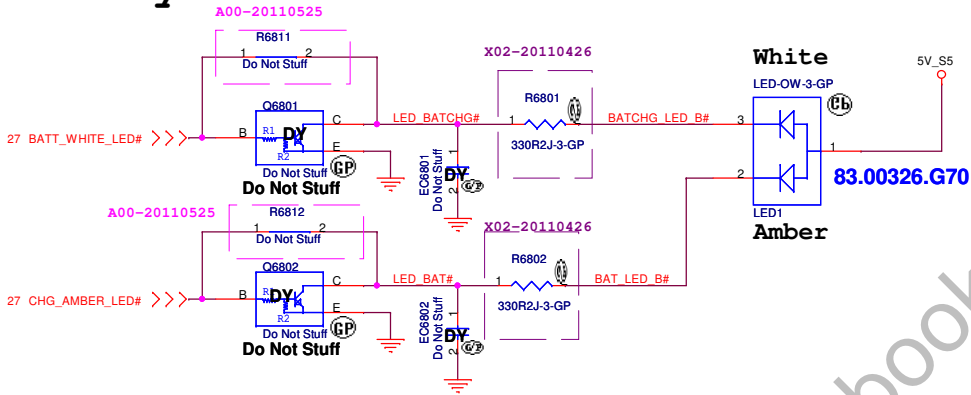
Power BTN Connector



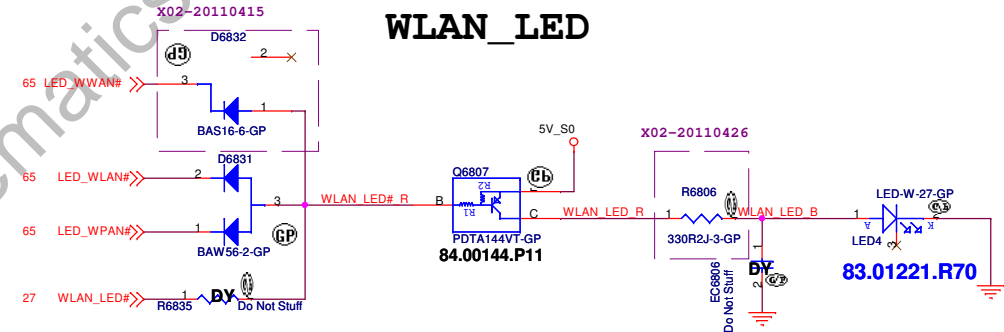
Power LED



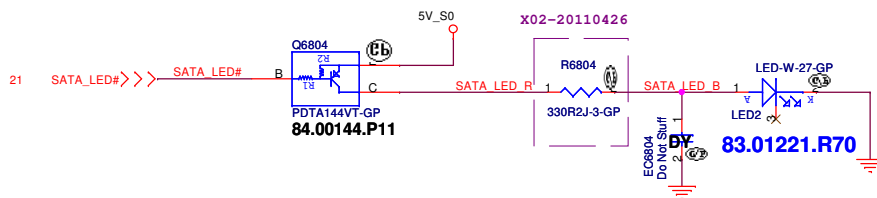
Battery LED



WLAN_LED



HDD LED



LED Location from left to right
(MB, Top View)

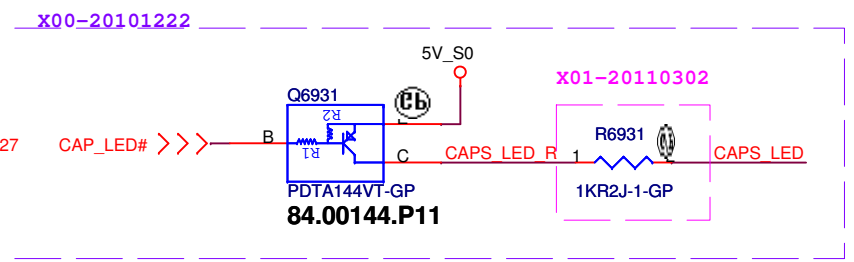
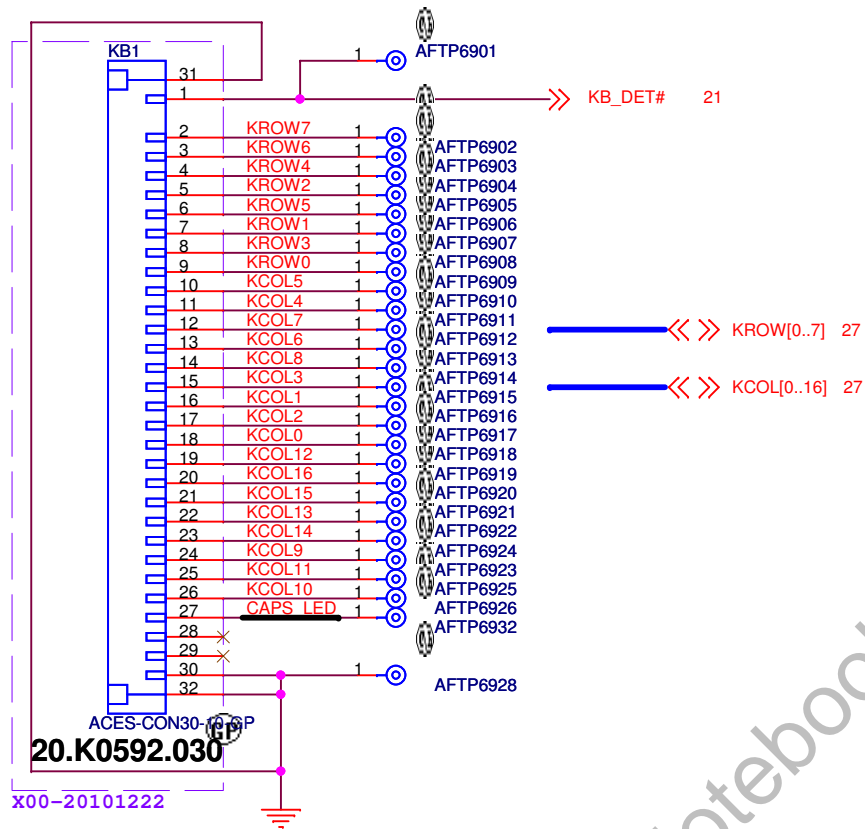


DV15 HR Vos GIGA HDMI NoSurge

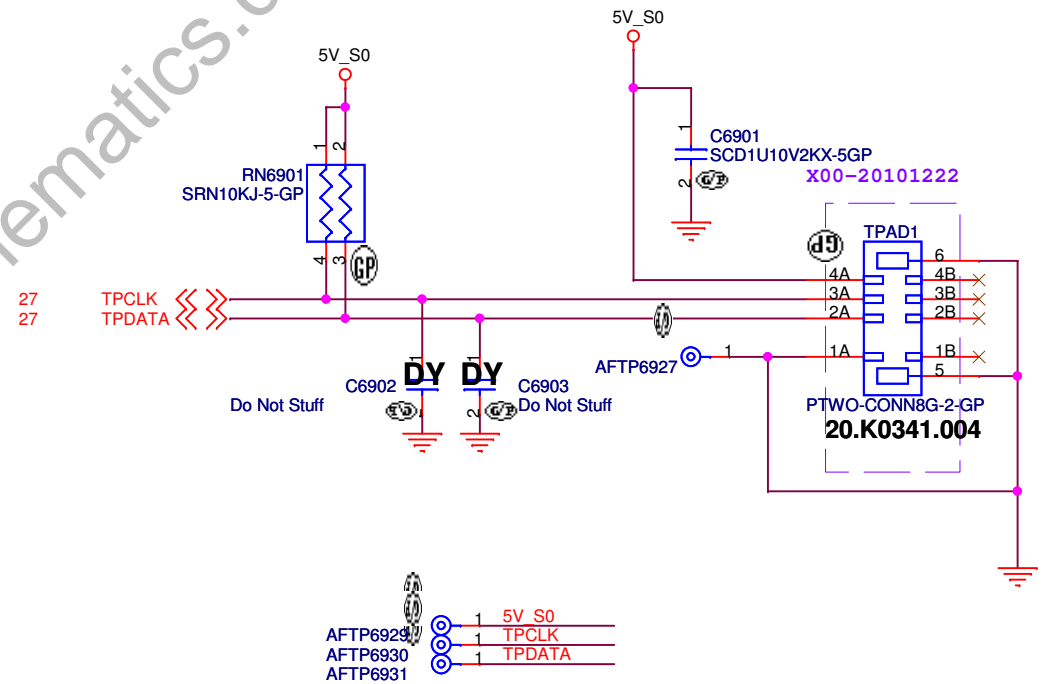
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Title LED Bard/Power Button		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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Internal KeyBoard Connector



TouchPad Connector



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Title		
Key Board/Touch Pad		
Size	Document Number	Rev
A4		X01
Enrico/Caruso 15 HR		
Date: Thursday, June 02, 2011	Sheet 69	of 104

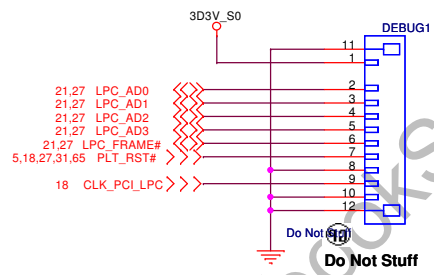
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Title		
Hall Sensor		
Size	Document Number	Rev
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Title		
Dubug connector		
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Reserved		
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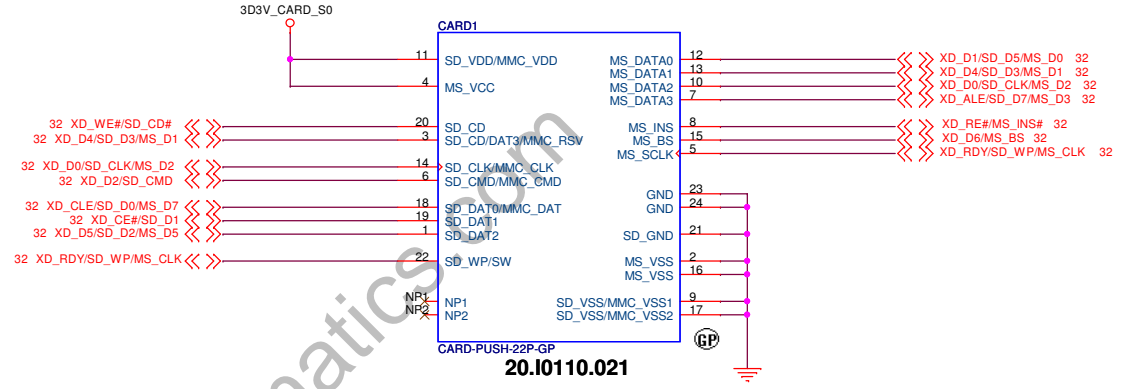
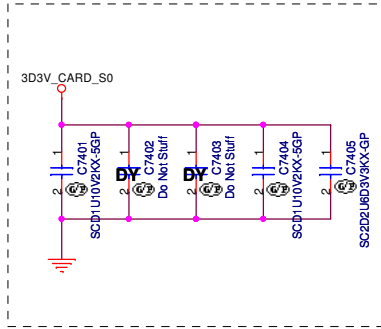
DV15 HR Vos GIGA HDMI NoSurge



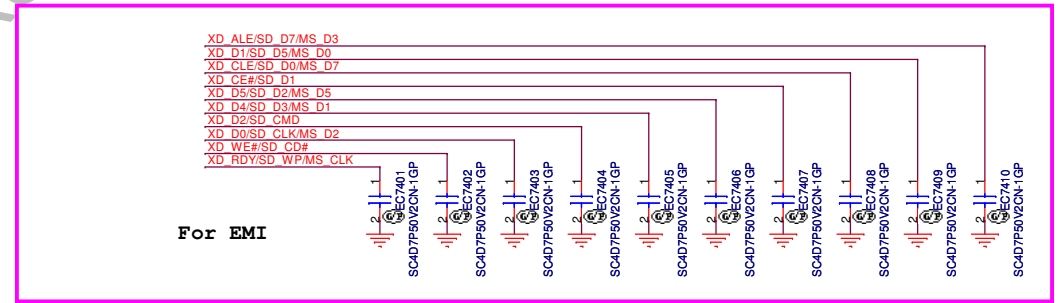
Title		
Reserved		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
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SSID = SDIO

SD/MMC/MS Card Reader



X01-20110315



For EMI

SSID = ExpressCard

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	Wistron Corporation	
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Title		
Express Card		
Size	Document Number	Rev
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Title		
Reserved		
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SSID = User.Interface

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Free Fall Sensor		
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Reserved		
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Title		
IO Board Connector		
Size	Document Number	Rev
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Title		
GPU PCIE/STRAPPING(1/5)		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
GPU Memory(2/5)		
Size	Document Number	Rev
Custom	Enrico/Caruso 15 HR	X01
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		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
GPU DP/LVDS/CRT/GPIO(3/5)			
File	Document Number		Rev
	Enrico/Caruso 15 HR		X01
Date:	11/25/11, June 12, 2011	Sheet	62 of 104

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.	
File			
GPU POWER(4/5)			
Size	Document Number	Rev	
K2	Enrico/Caruso 15 HR	X01	
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Title		
GPU-VRAM1,2 (1/4)		
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
GPU-VRAM3,4 (2/4)					
Size	Document Number				Rev
Custom	Enrico/Caruso 15 HR				X01
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Title		
GPU-VRAM5,6 (3/4)		
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		GPU-VRAM7,8 (4/4)	
Size A3	Document Number	Rev	X01
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
RT8208B +VGA CORE		
Size	Document Number	Rev
A3	Enrico/Caruso 15 HR	X01
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LVDS Switch			
Size	Document Number	Rev	
A3	Enrico/Caruso 15 HR	X01	
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT Switch			
Size	Document Number	Rev	
A3	Enrico/Caruso 15 HR	X01	
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SSID = SDIO

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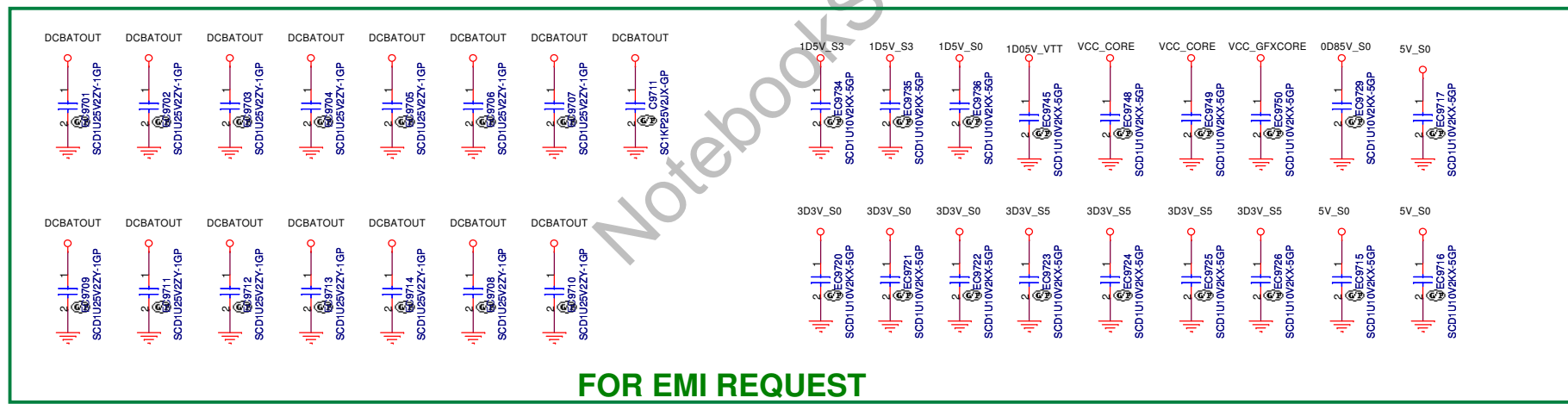
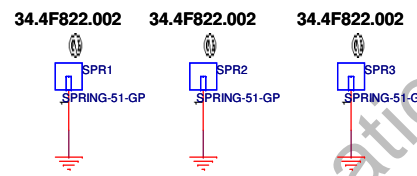
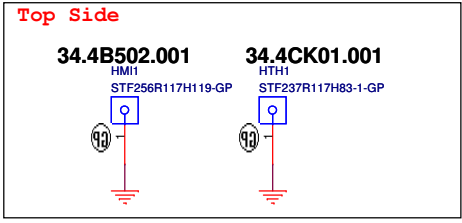
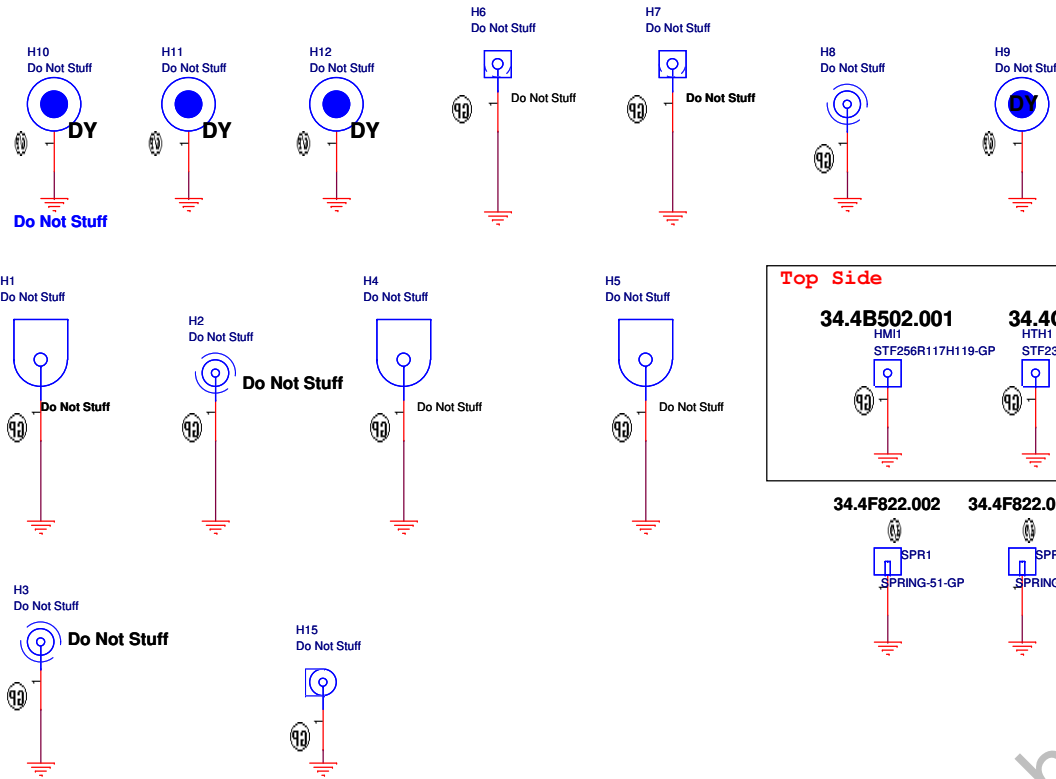
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Title		
TOUCH PANEL		
Size	Document Number	Rev
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SSID = Mechanical



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Title: **UNUSED PARTS/EMI Capacitors**

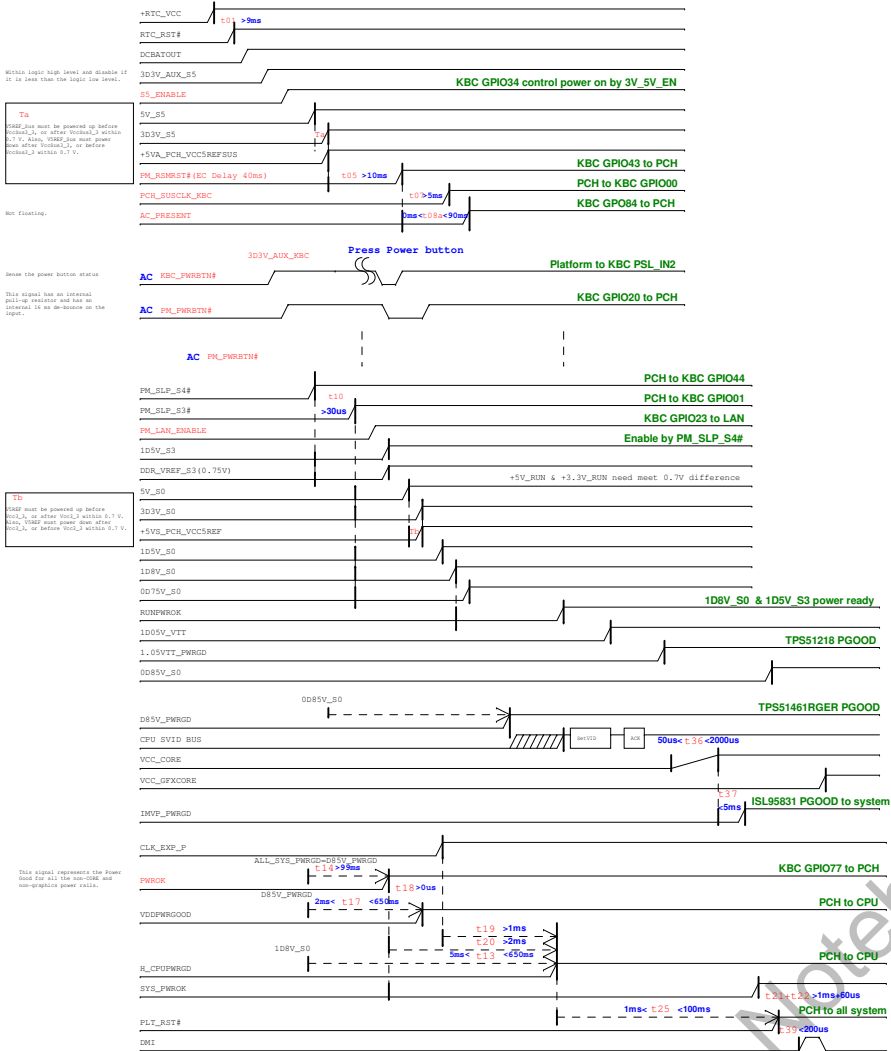
Size A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

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Huron River Platform Power Sequence

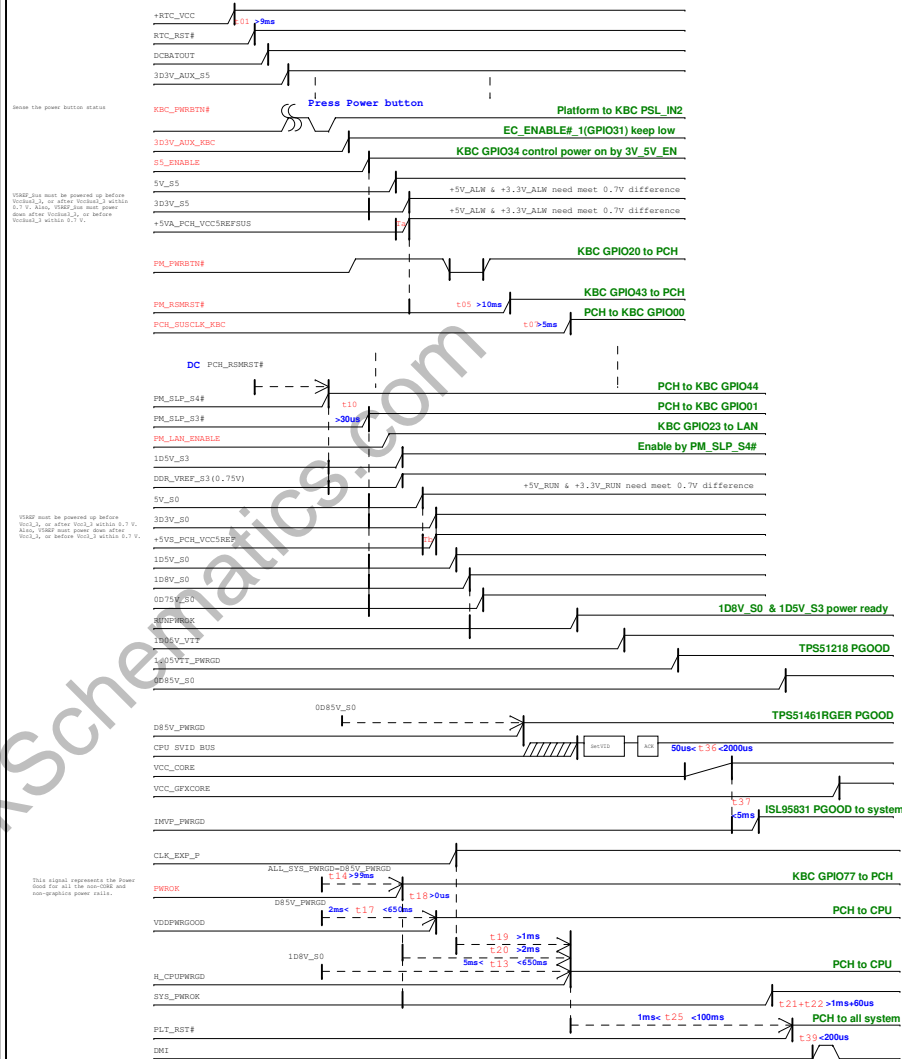
(AC mode)

red word: KBC GPIO

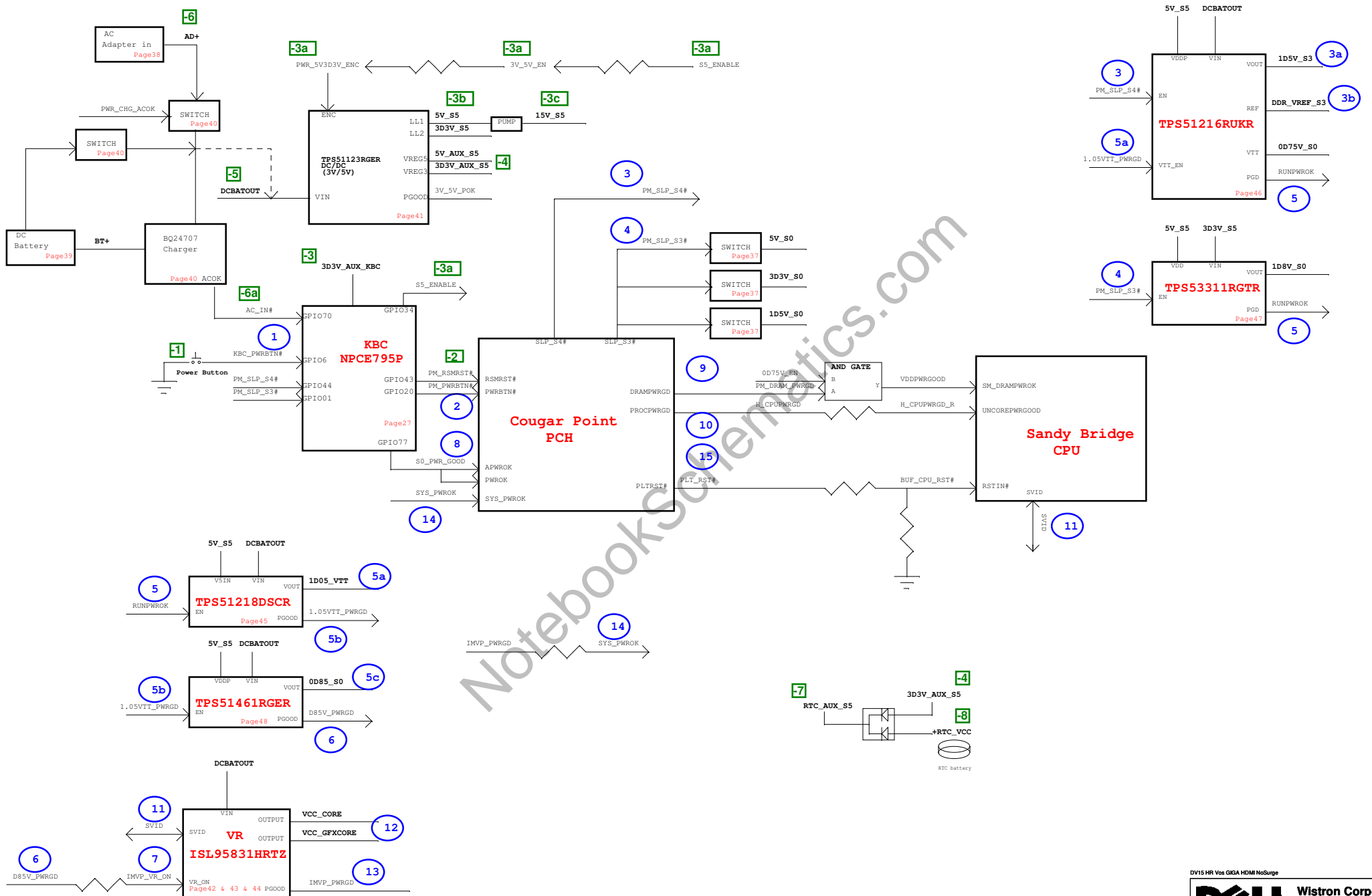


(DC mode)

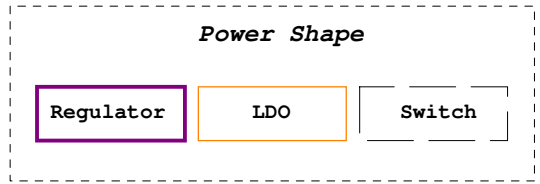
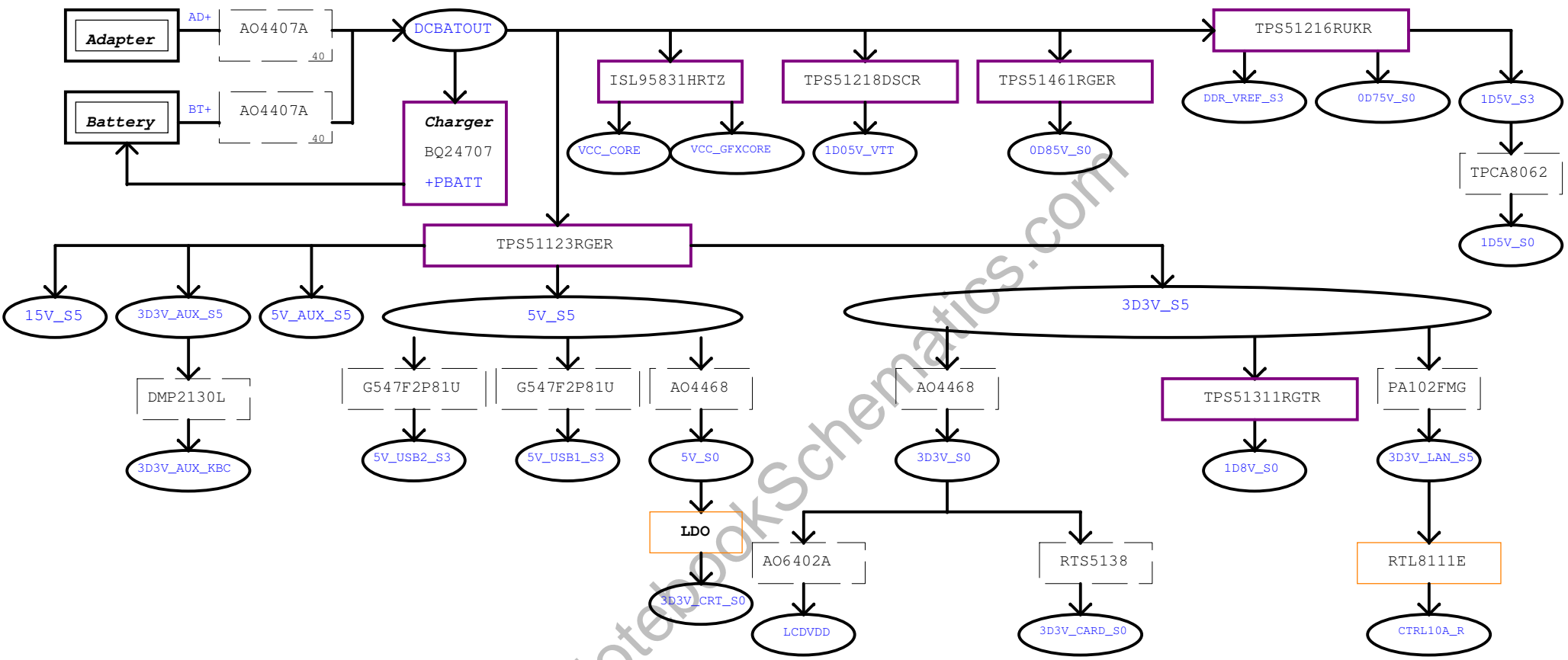
red word: KBC GPIO



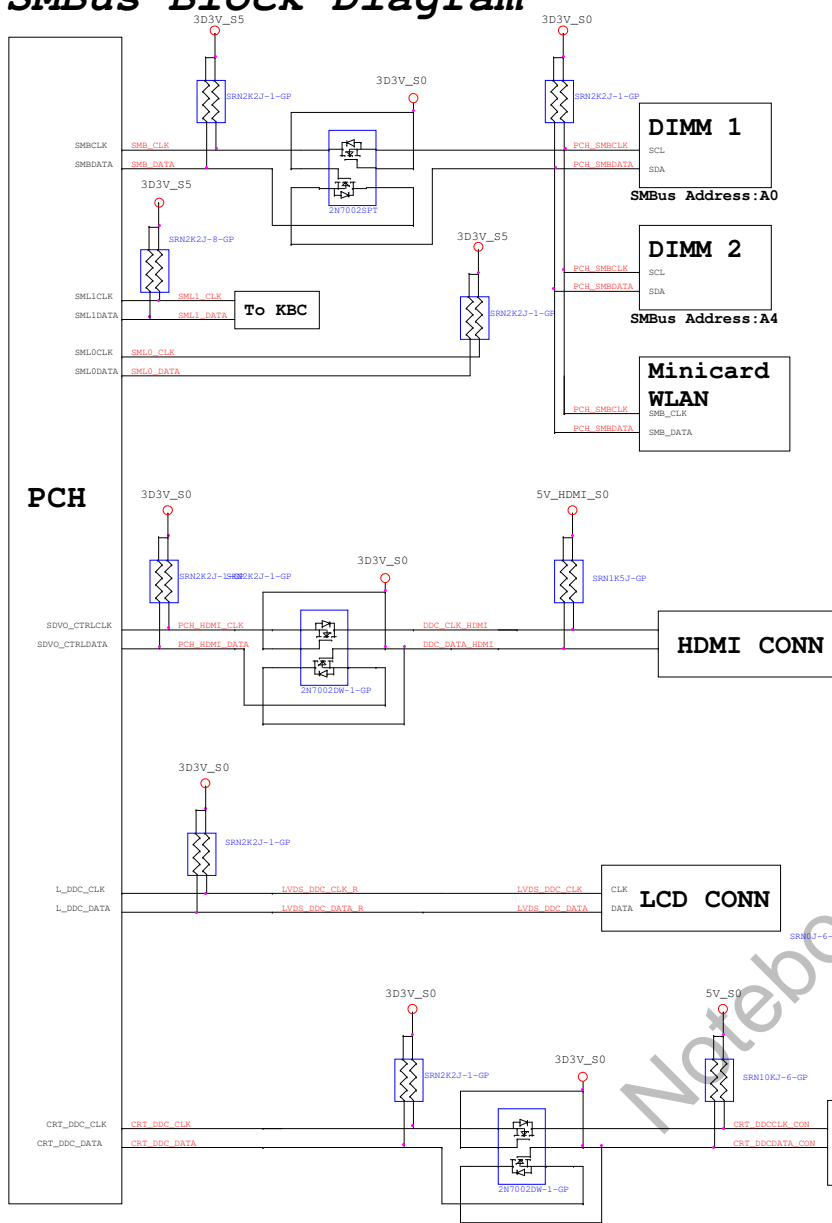
Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



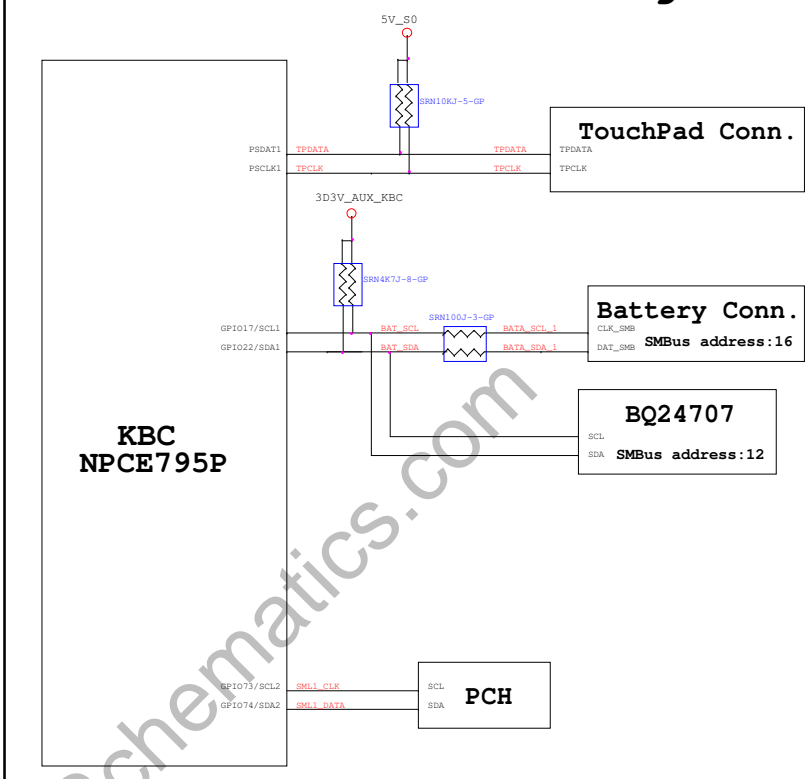
Power Up Sequence: **-8** ~ **15**



PCH SMBus Block Diagram



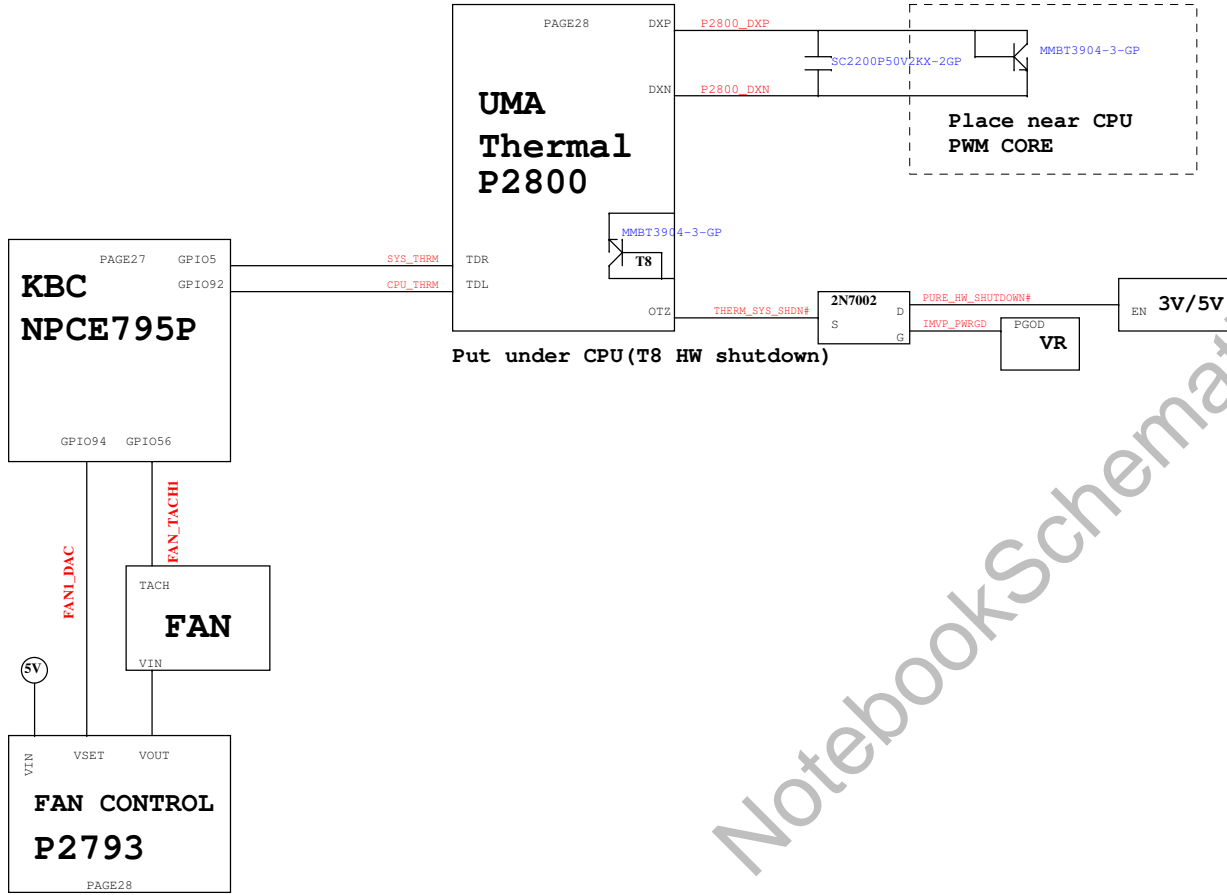
KBC SMBus Block Diagram



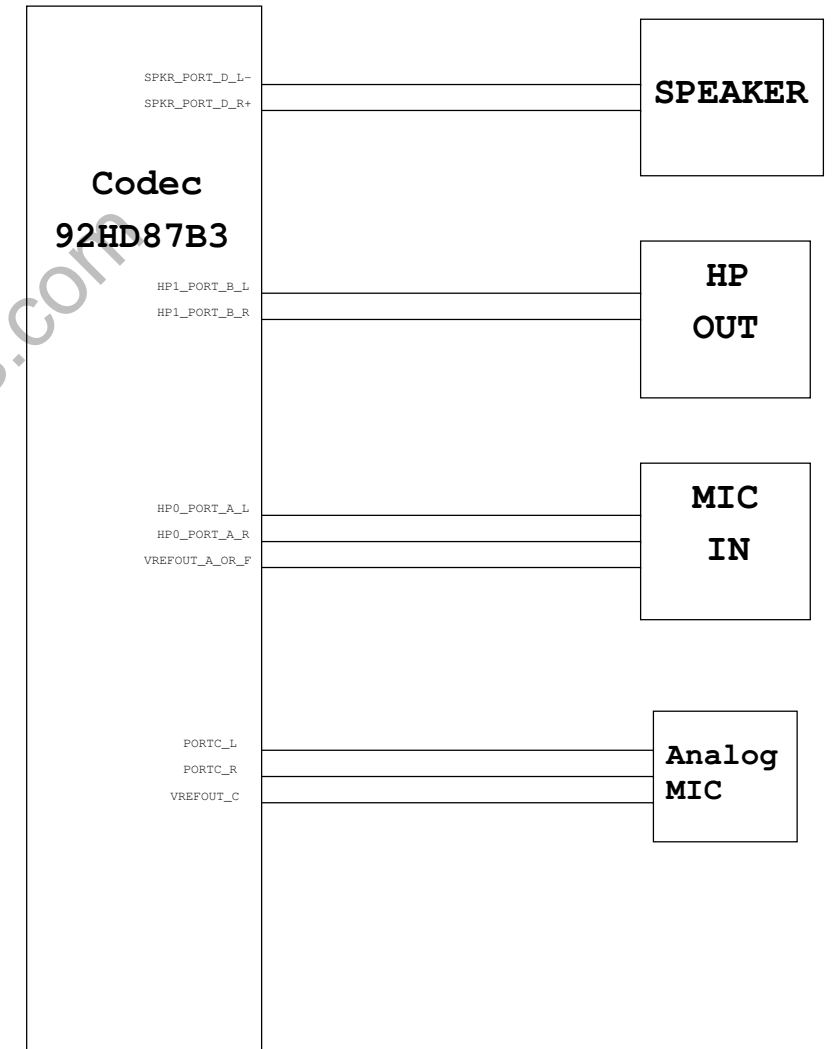
PCH

KBC
NPCE795P

Thermal Block Diagram



Audio Block Diagram



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